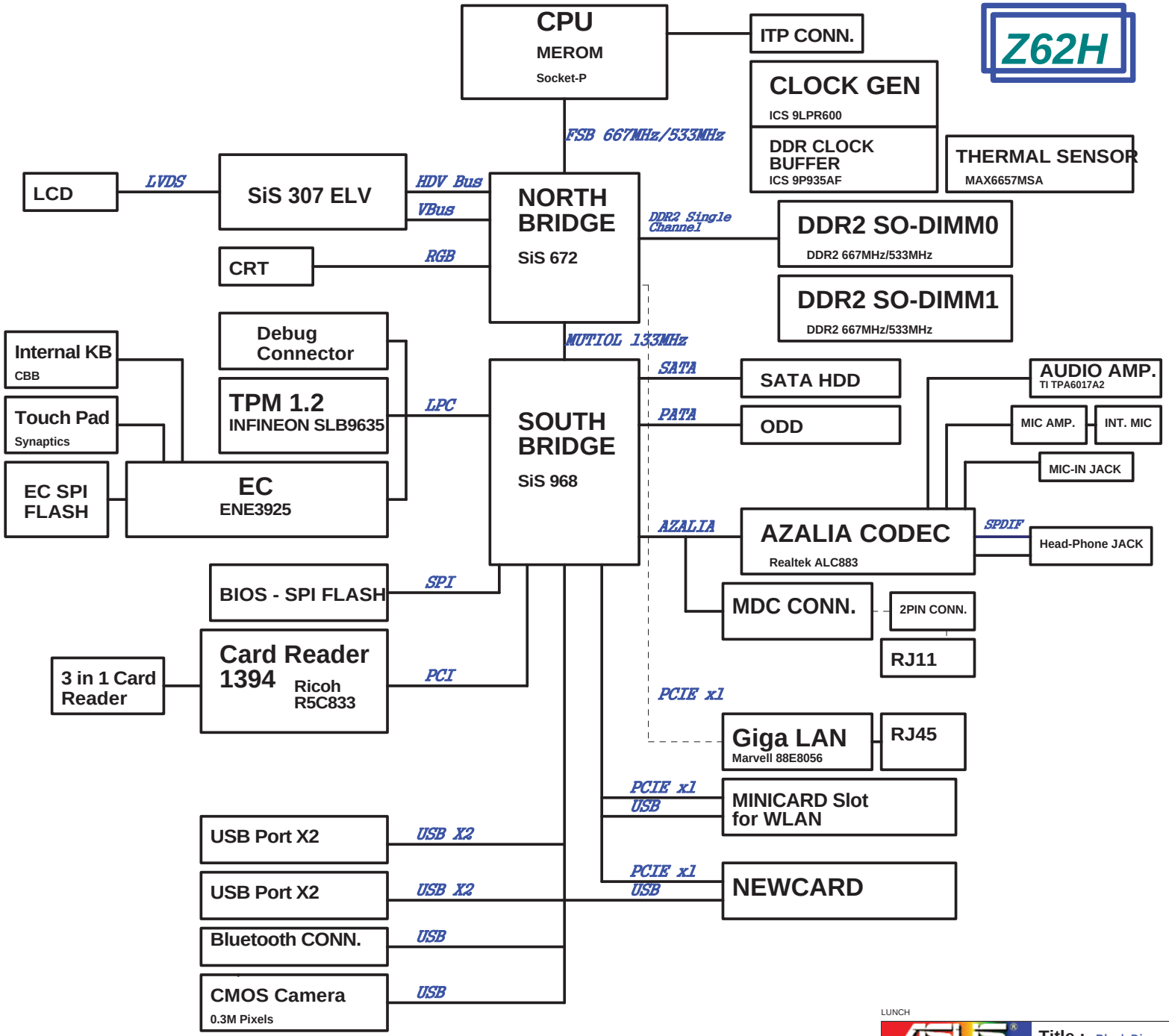


LUNCH

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 1 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

LUNCH

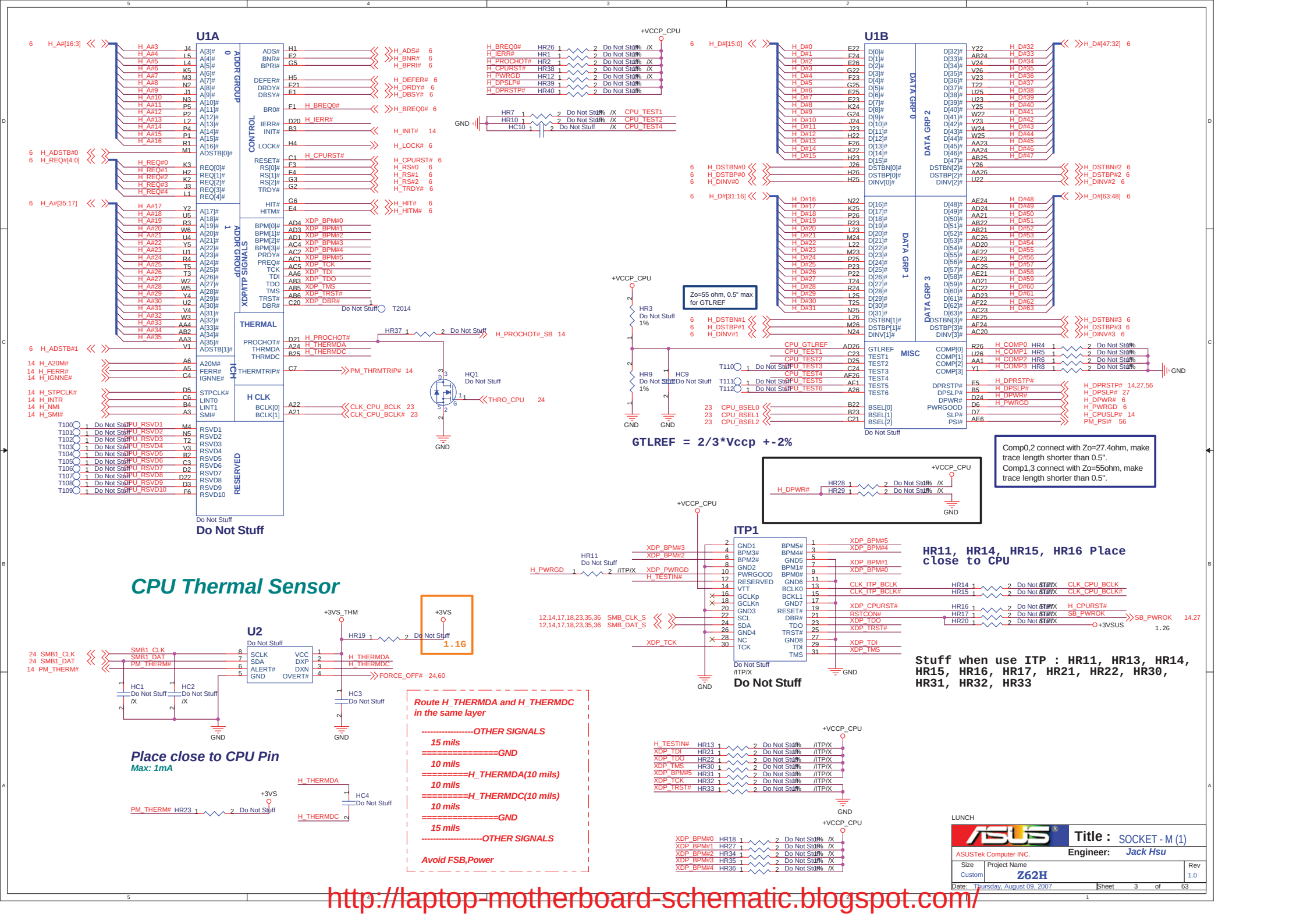
ASUSTek Computer INC.

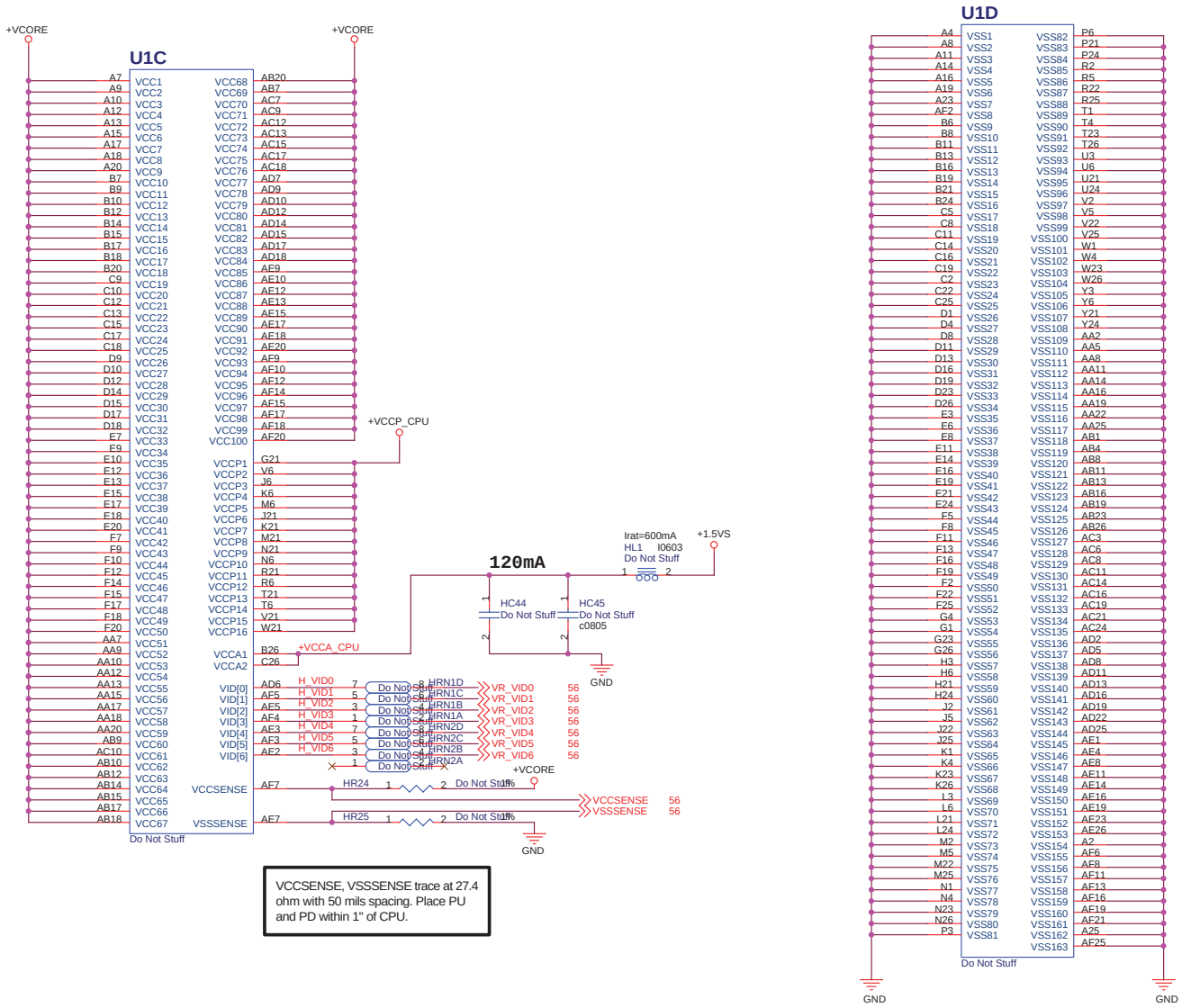
Title : System Setting

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 2 of 63

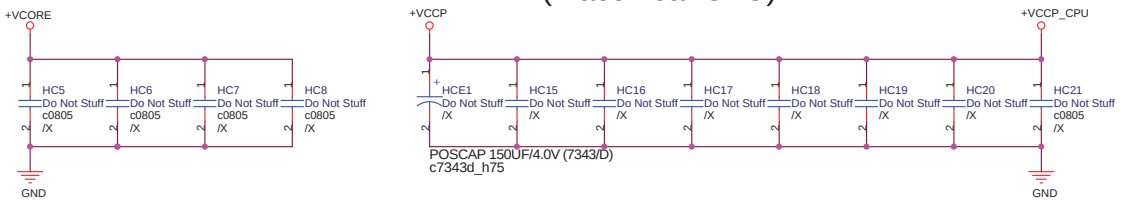




LUNCH

Title :	SOCKET - M (2)
ASUSTek Computer INC.	Engineer: Jack Hsu
Size: Custom	Project Name: Z62H
Rev: 1.0	
Date: Thursday, August 09, 2007	Sheet 4 of 63

+VCCP Decoupling Capacitor (Place near CPU)



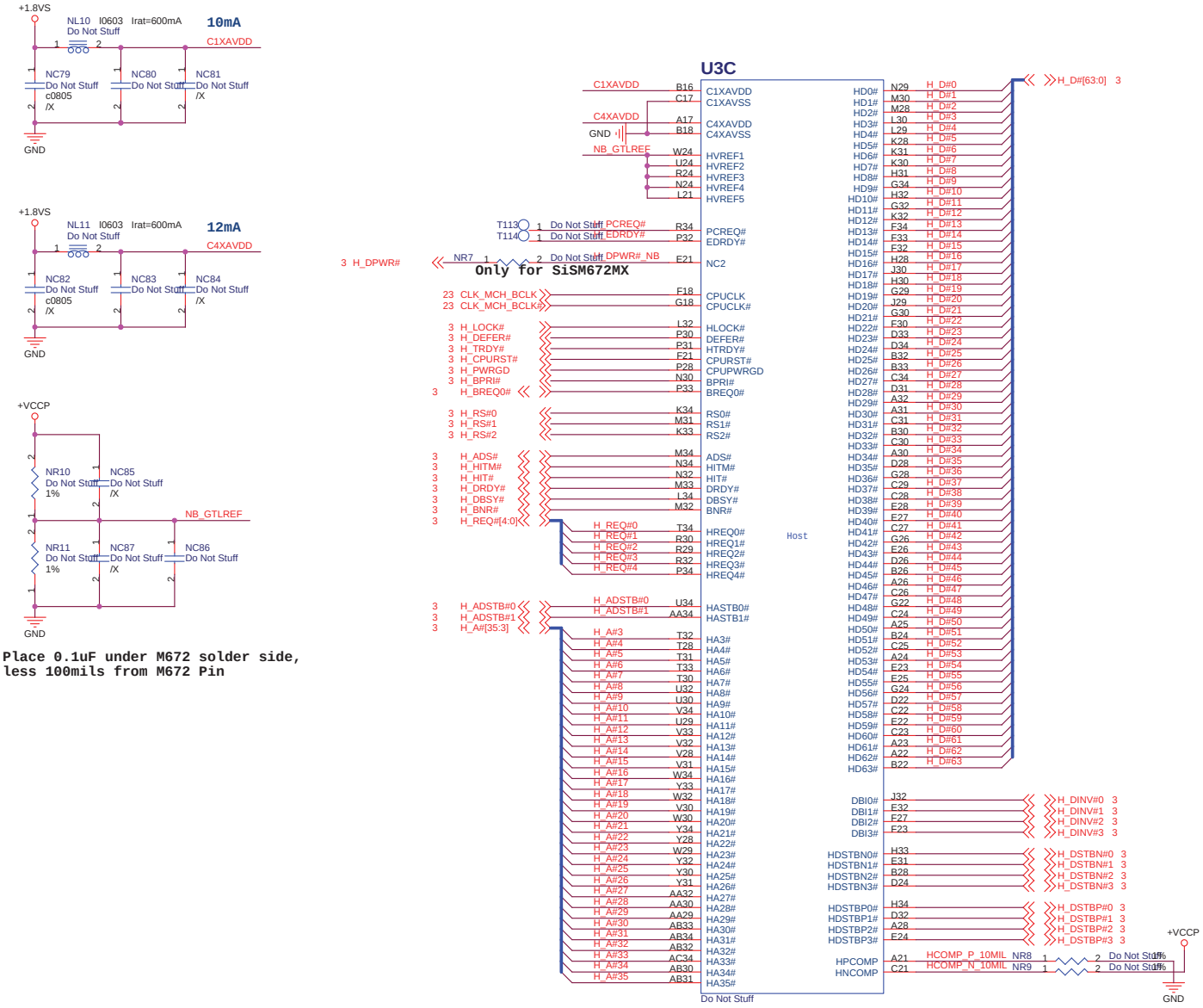
Non-Stuff

Decoupling guide from INTEL
44A for Merom

VCORE 22uF/10V * 32pcs, 330uF/2V * 6pcs
VCCP 0.1uF * 6pcs, 150uF * 1pcs

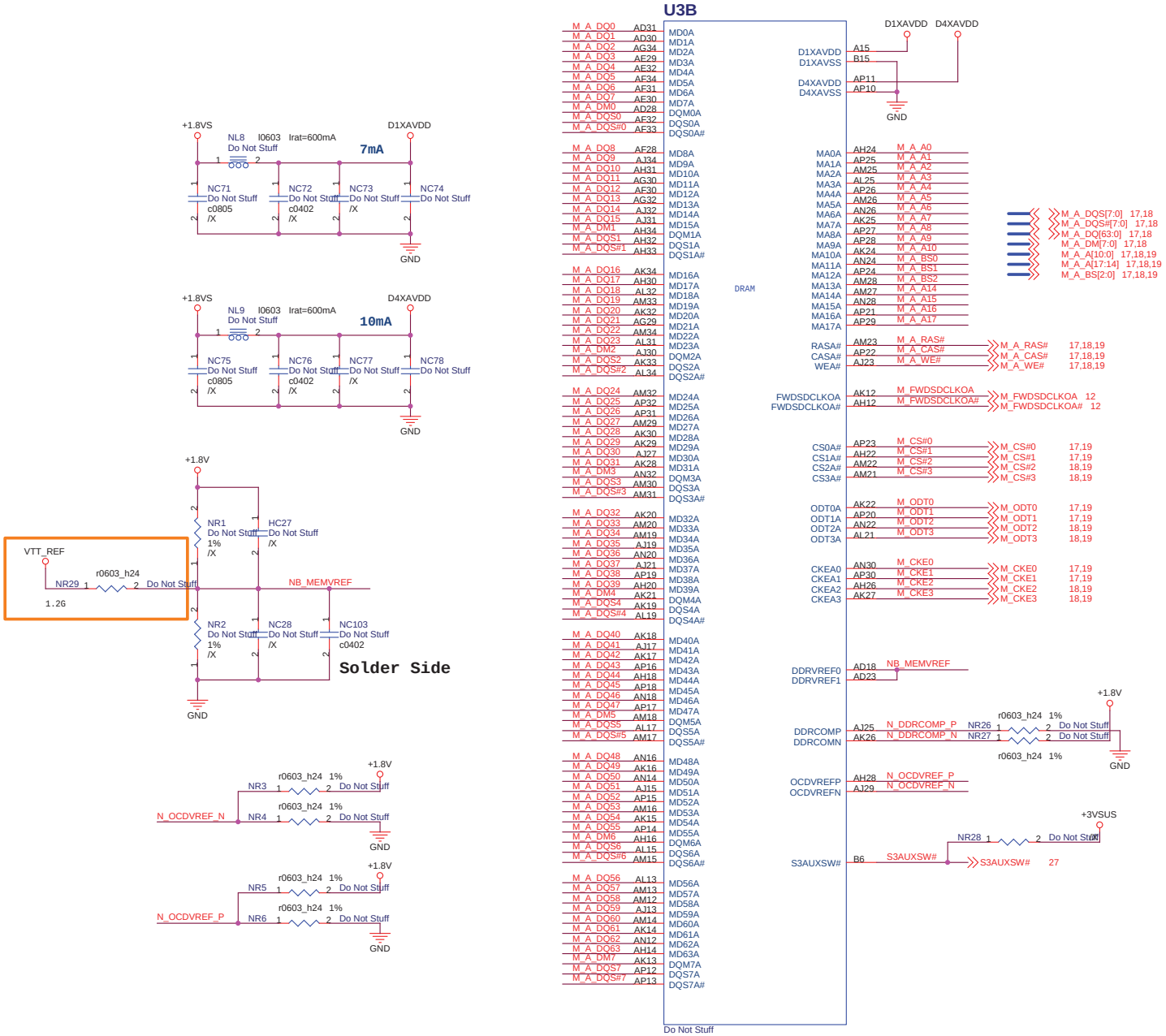
LUNCH

ASUSTek Computer INC.	Title : CPU CAP	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 5 of 63	



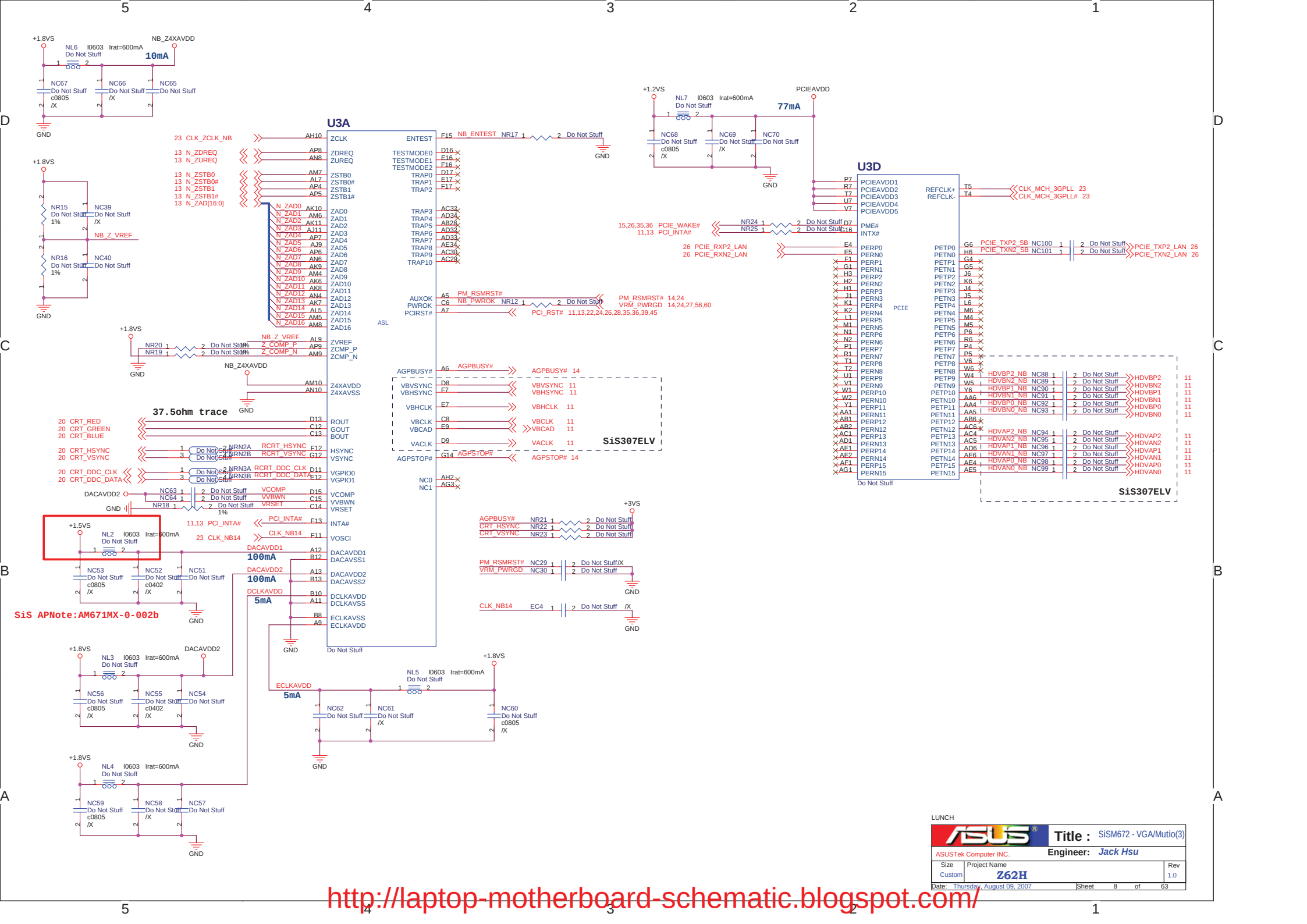
LUNCH

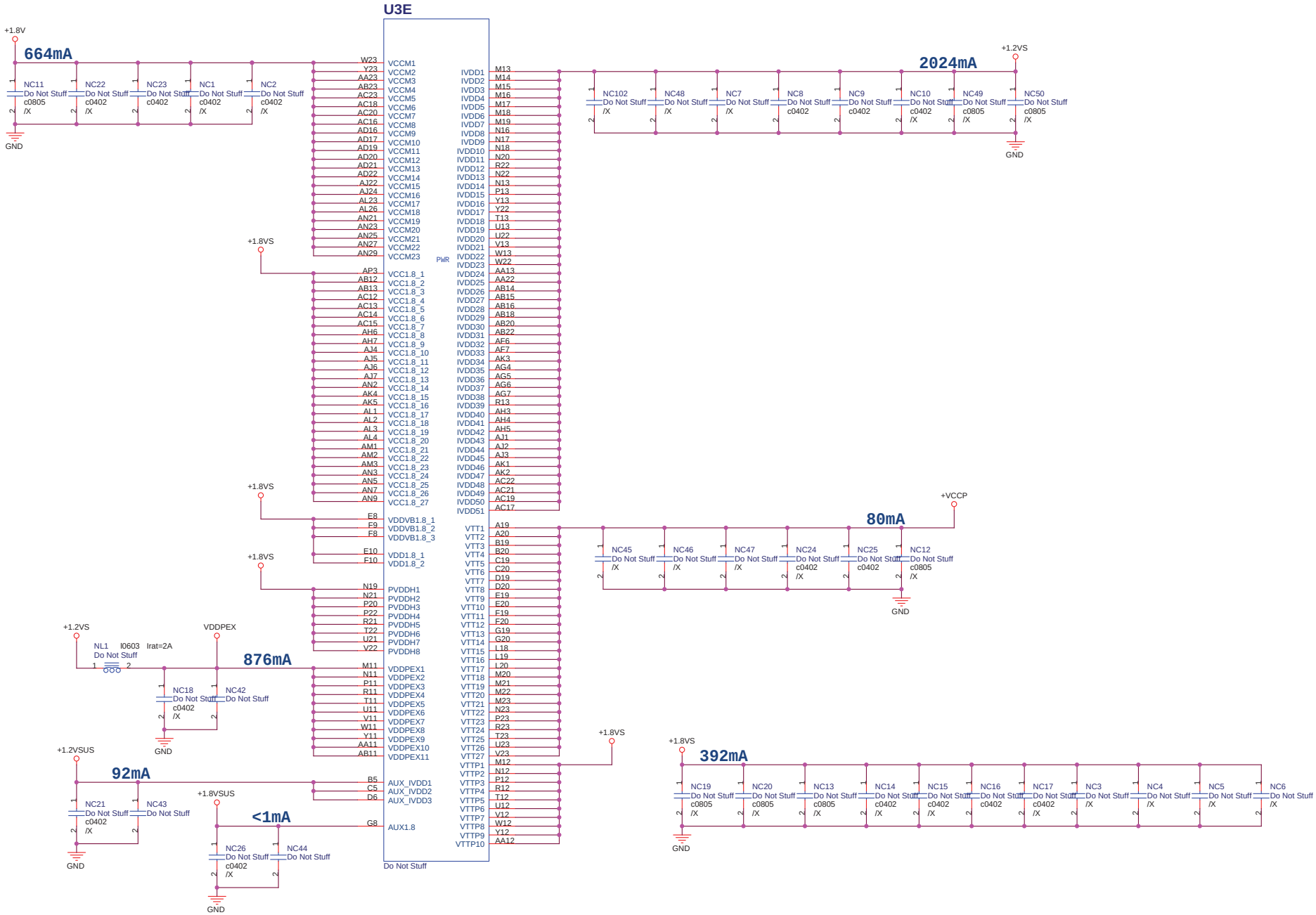
ASUSTek Computer INC.	Title : SiSM672 - HOST(1)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 6 of 63	



LUNCH

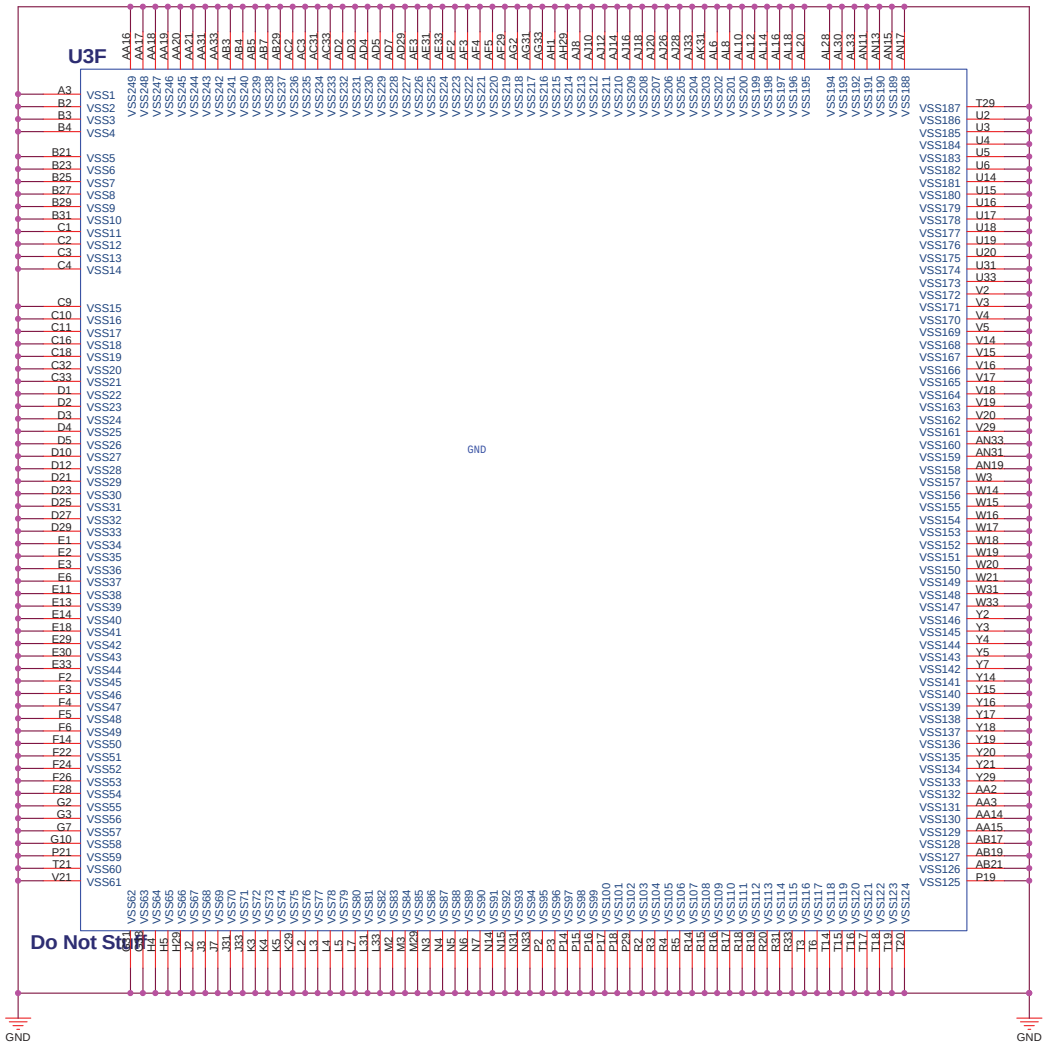
ASUSTek Computer INC.	Title : SiSM672 - DDR2(2)		
	Engineer: Jack Hsu		
Size: Custom	Project Name: Z62H		Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 7 of 63		


U3A
U3D
SiS307ELV
SiS307ELV
37.5ohm trace
SiS APNote:AM671MX-0-002b
10mA
77mA
100mA
100mA
5mA
5mA
LUNCH
Title : SiSM672 - VGA/Mutio(3)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 8 of 63
http://laptop-motherboard-schematic.blogspot.com/



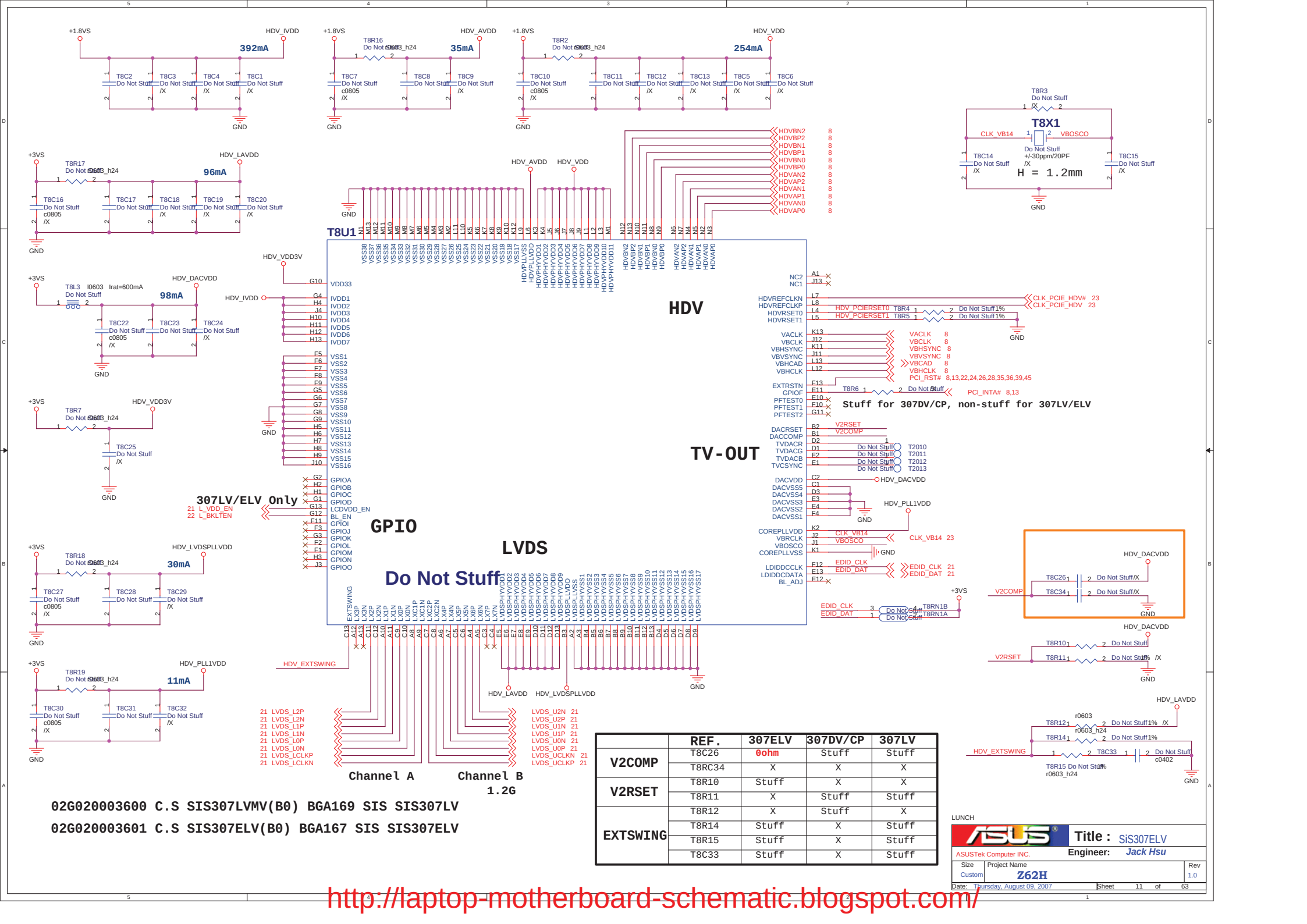
LUNCH

ASUSTek Computer INC.	Title : SiSM672 - POWER(4)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 9 of 63	



LUNCH

ASUSTek Computer INC.	Title : SiSM672 - GND(5)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 10 of 63	



	REF.	307ELV	307DV/CP	307LV
V2COMP	T8C26	0ohm	Stuff	Stuff
	T8RC34	X	X	X
V2RSET	T8R10	Stuff	X	X
	T8R11	X	Stuff	Stuff
EXTSWING	T8R12	X	Stuff	X
	T8R14	Stuff	X	Stuff
	T8R15	Stuff	X	Stuff
	T8C33	Stuff	X	Stuff

LUNCH

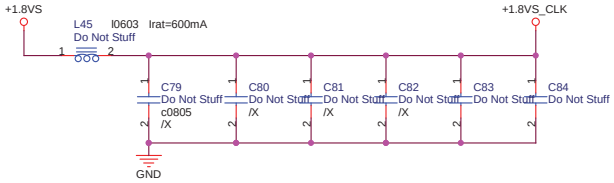
ASUSTek Computer INC.

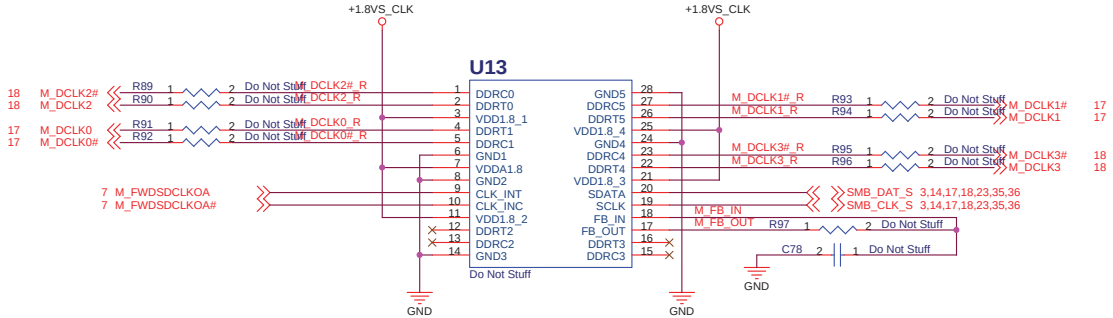
Title : SiS307ELV

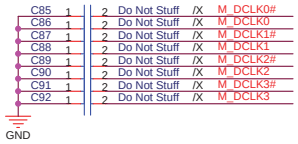
Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 11 of 63

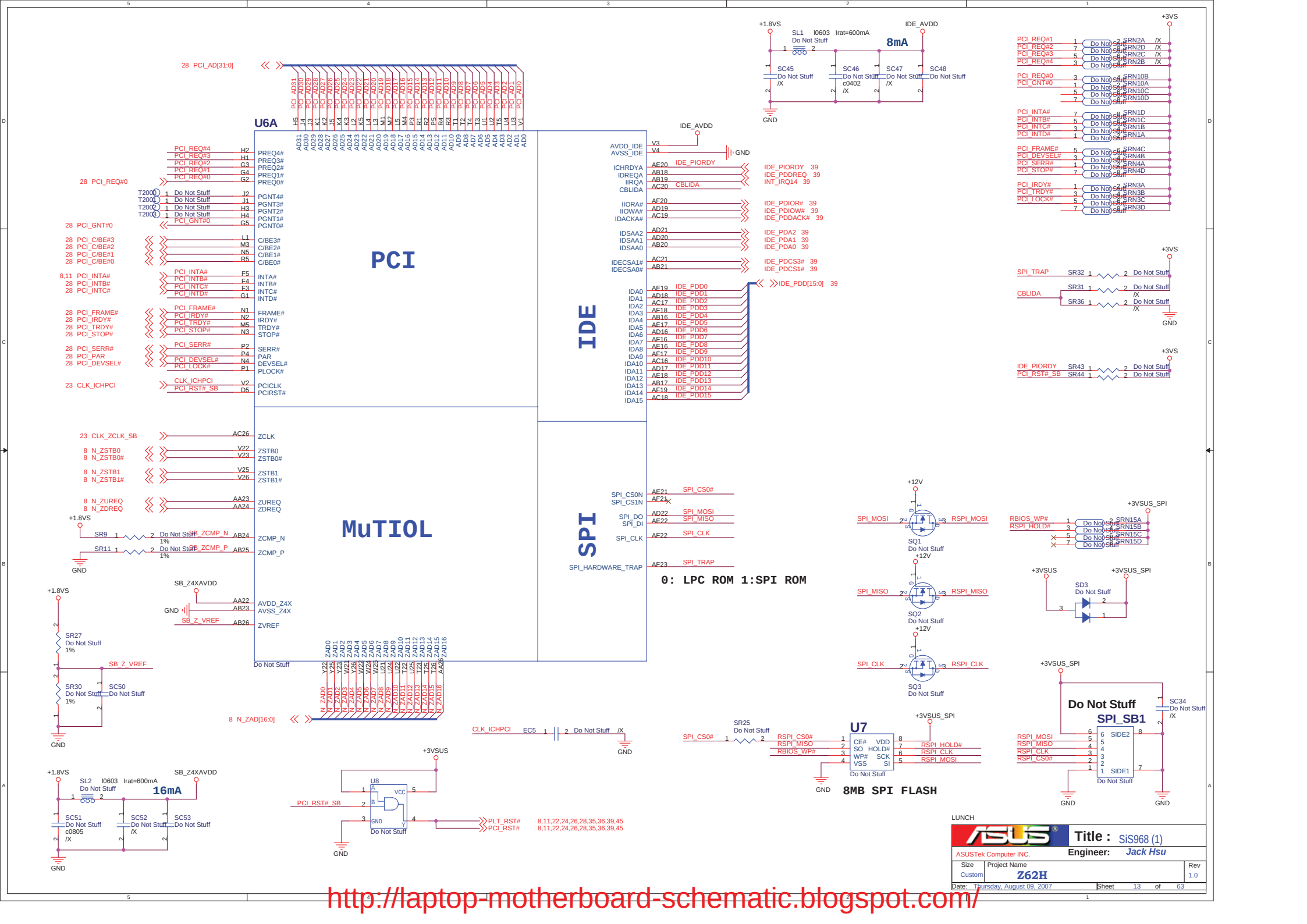


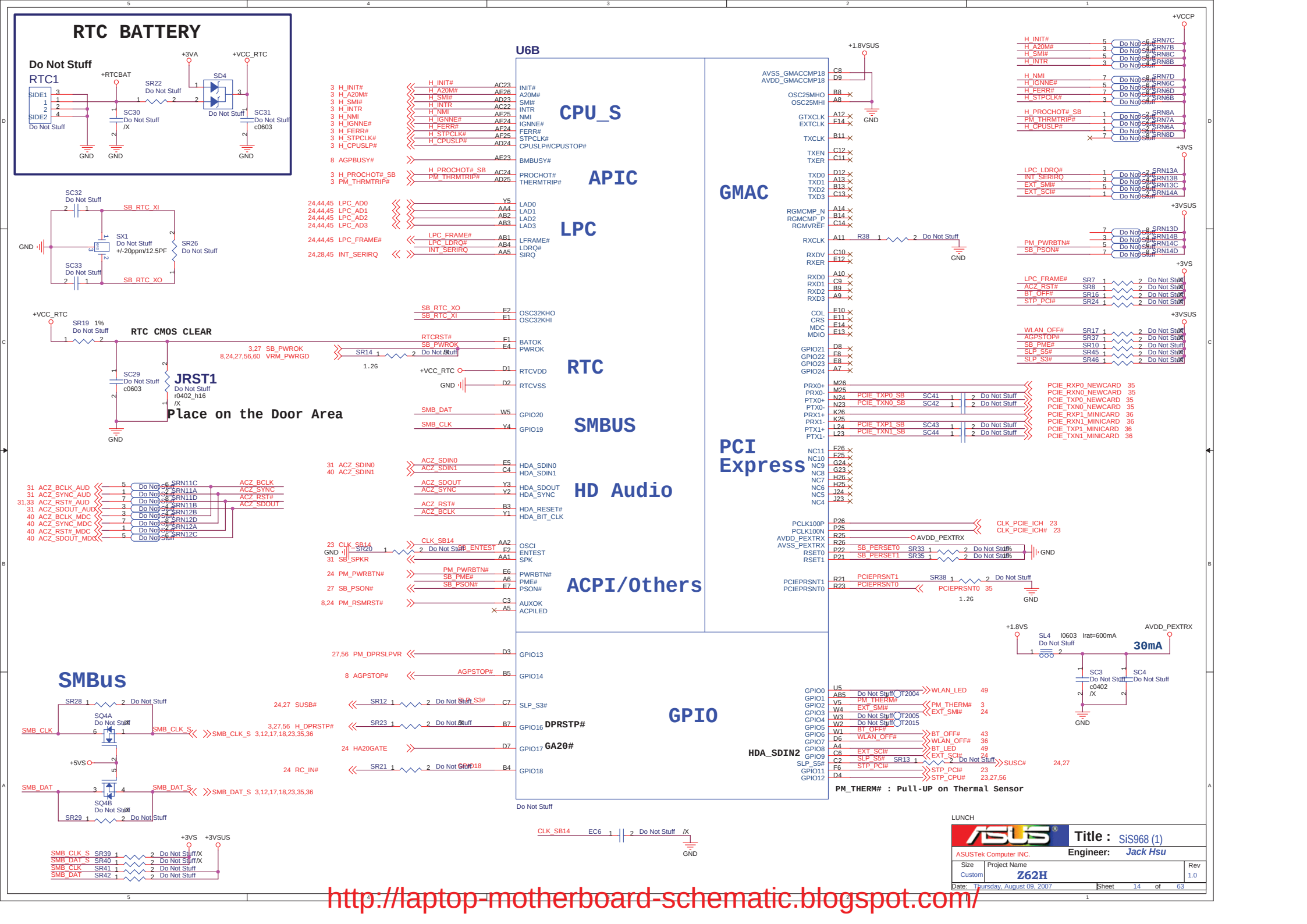




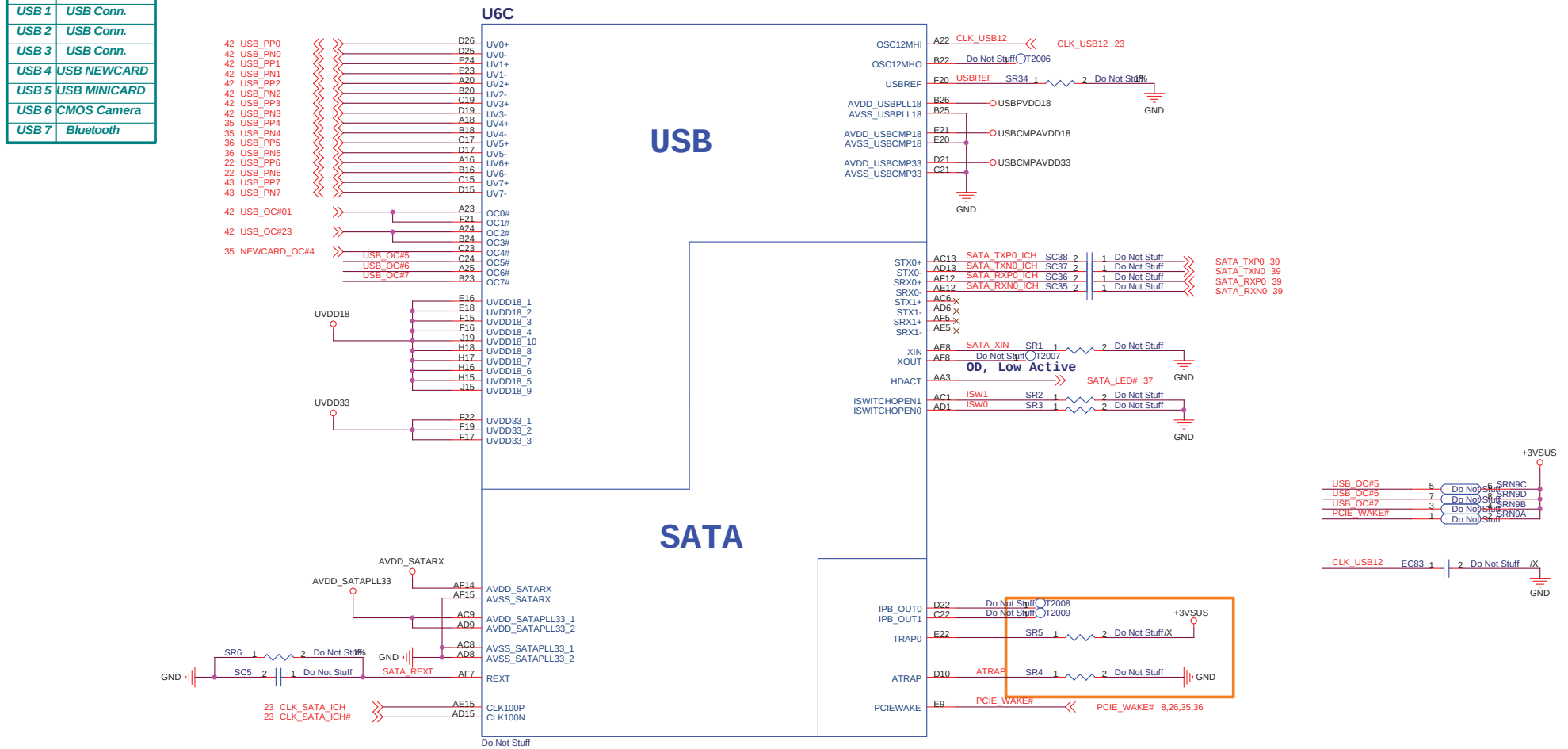
LUNCH

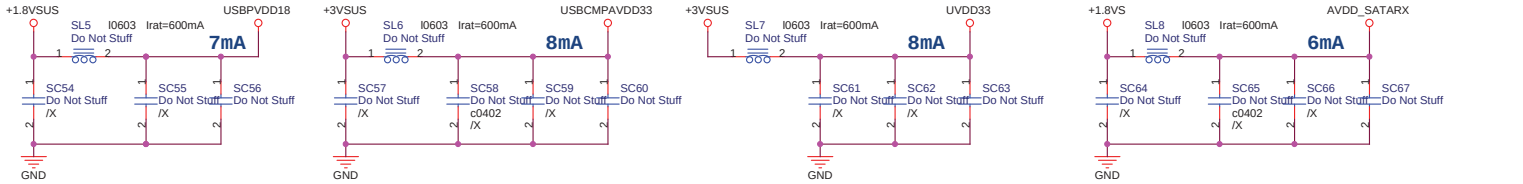
ASUSTek Computer INC.	Title : DDR2 CLOCK BUFFER		
	Engineer: Jack Hsu		
Size: Custom	Project Name: Z62H		Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 12 of 63		

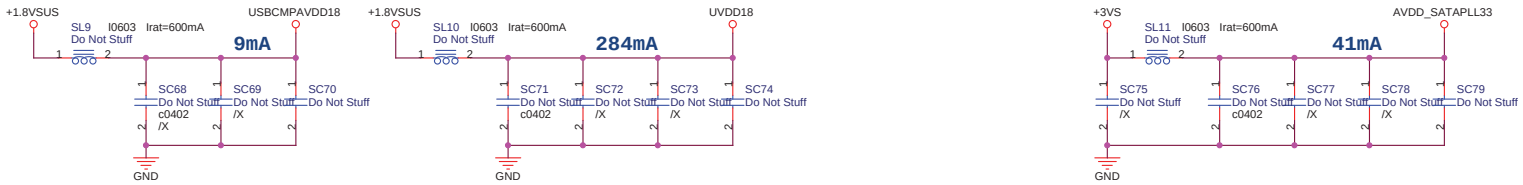



RTC BATTERY
Do Not Stuff
RTC1
SIDE1
SIDE2
+RTCBAT
+3VA
+VCC_RTC
SD4
SR22
SC30
SC31
GND
U6B
CPU_S
APIC
LPC
RTC
SMBUS
HD Audio
ACPI/Others
GPIO
GMAC
PCI Express
SMBus
SC32
SX1
SR26
SC33
SB_RTC_XI
SB_RTC_XO
RTC CMOS CLEAR
SR19
SC29
JRST1
Place on the Door Area
SR14
1.26
+1.8VSUS
+VCCP
+3VS
+3VSUS
SR38
SR33
SR35
SL4
30mA
SC3
SC4
SQ4A
SQ4B
SR28
SR29
SR12
SR23
SR21
SR20
SR13
SUSC#
PM_THERM# : Pull-UP on Thermal Sensor
Do Not Stuff
LUNCH
Title : SiS968 (1)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 14 of 63
http://laptop-motherboard-schematic.blogspot.com/

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth

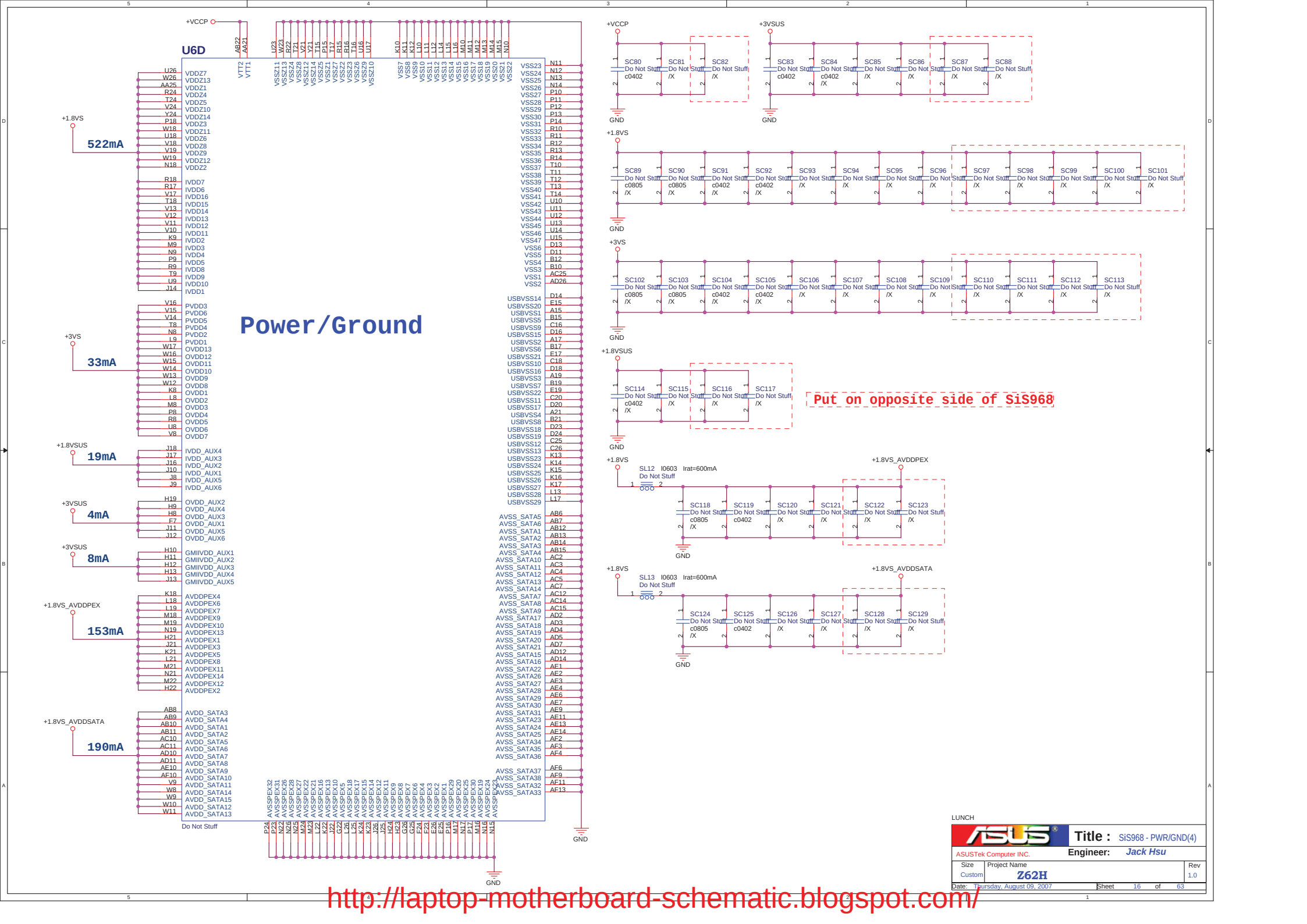


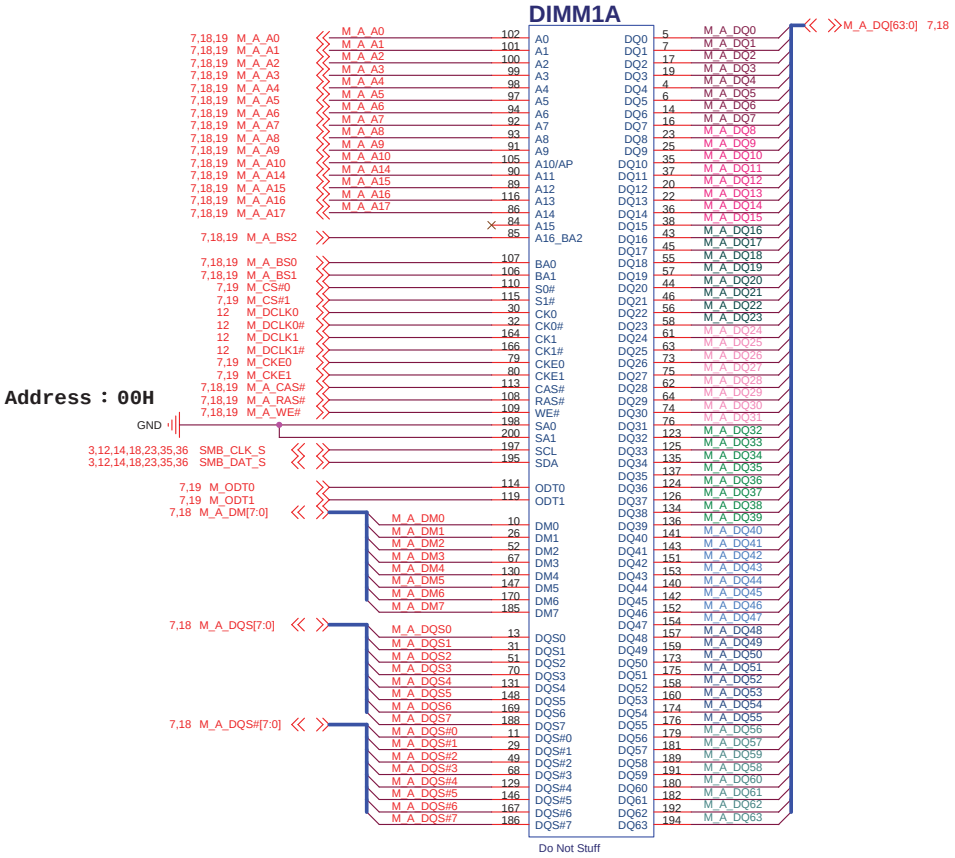


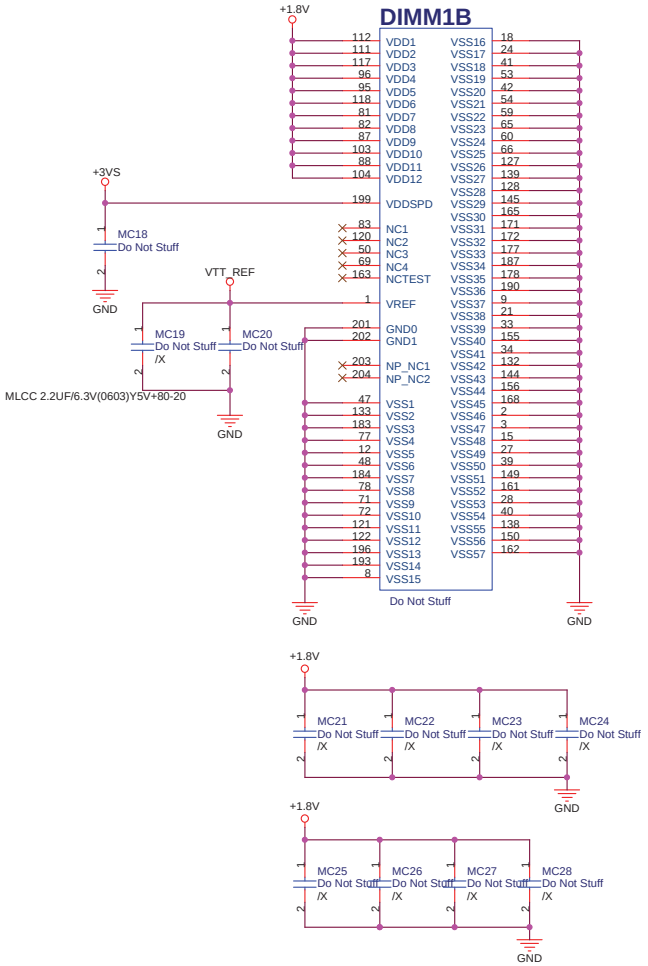


LUNCH

ASUSTek Computer INC.	Title : SiS968 (3)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 15 of 63	







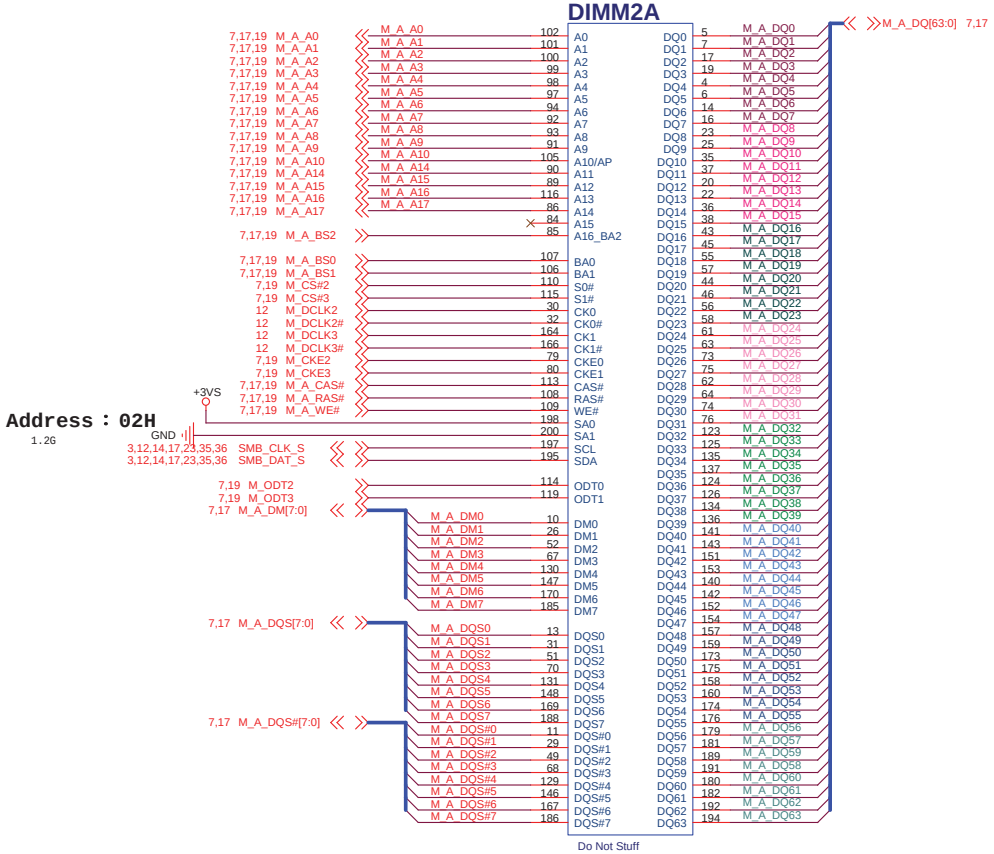
Layout Note: Place these Caps near SO-DIMM0

H=9.2mm Standard Type, 12G025C22000

Channel A, DIMM 0

LUNCH

ASUSTek Computer INC.	Title : DDR SO-DIMM0	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 17 of 63	

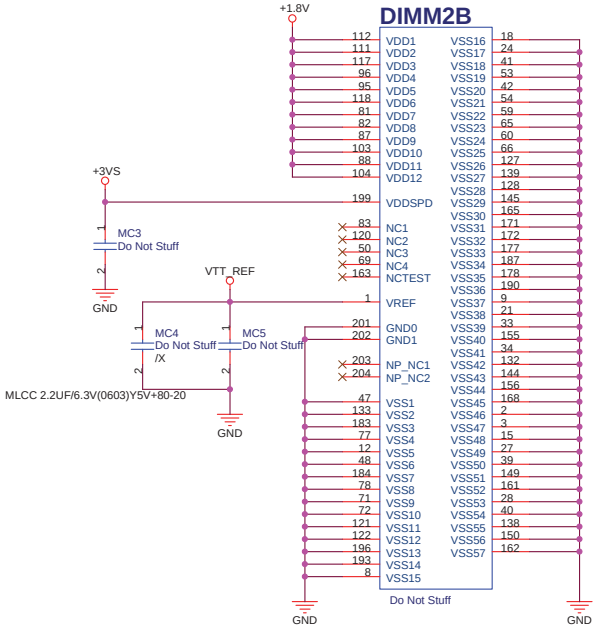


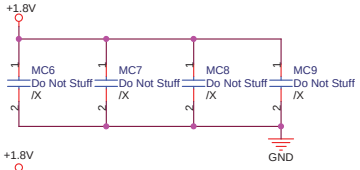
Address : 02H

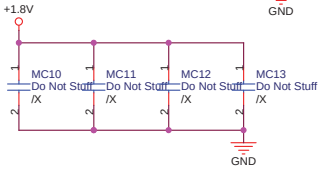
1.2G

H=5.2mm Standard Type, 12G025122007

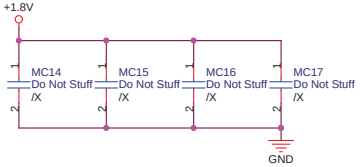
Channel A, DIMM 1







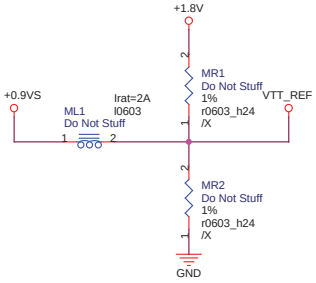
Layout Note: Place these Caps near SO-DIMM1

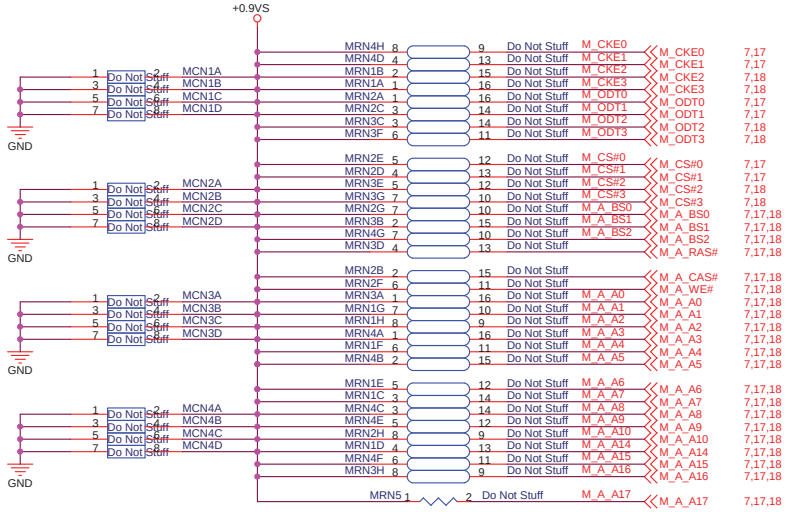


Layout Note: Place these High-Freq decoupling Caps near the GMCH

LUNCH

ASUSTek Computer INC.	Title : DDR SO-DIMM1	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 18 of 63	



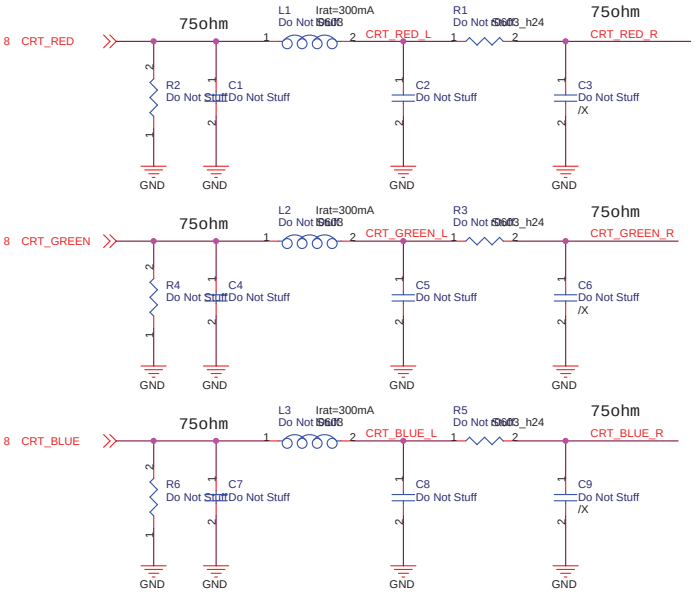


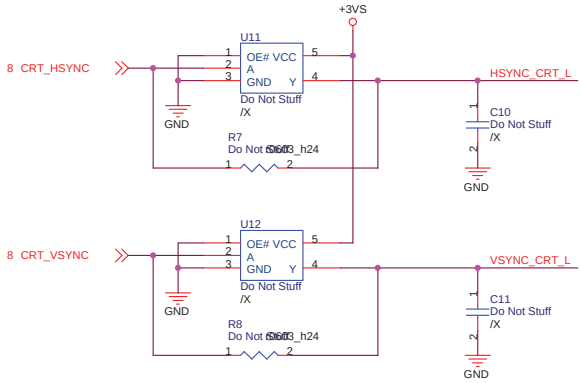
DDR2: Command, Control Signal need termination

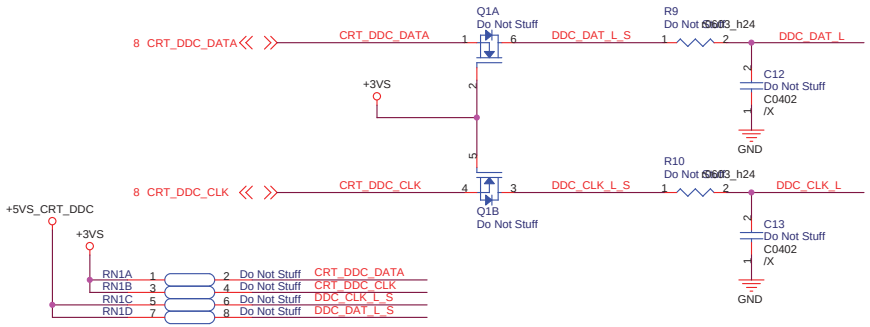
Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V

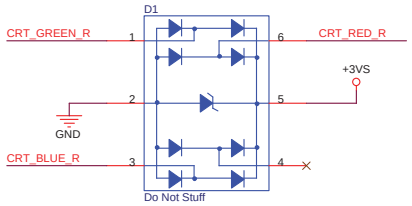
LUNCH

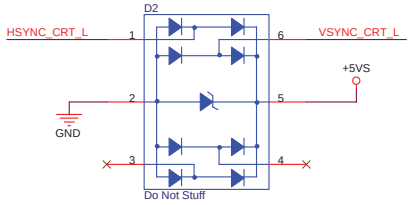
ASUSTek Computer INC.	Title : DDR2 Termination	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 19 of 63	





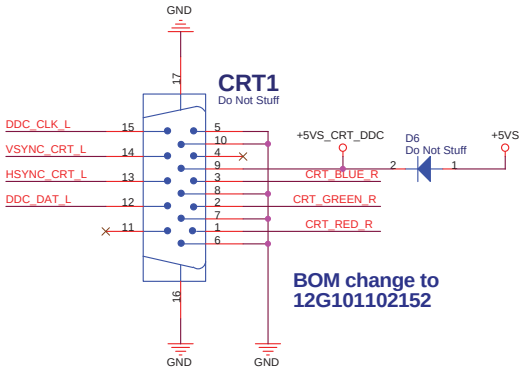






ESD Diodes

Place ESD Diodes near CRT Connector

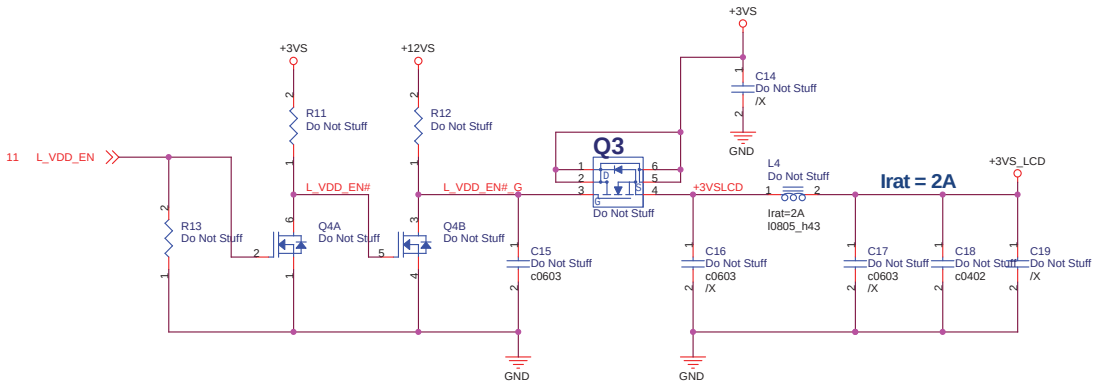


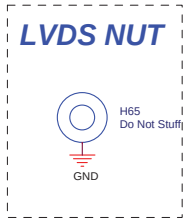
CRT Connector

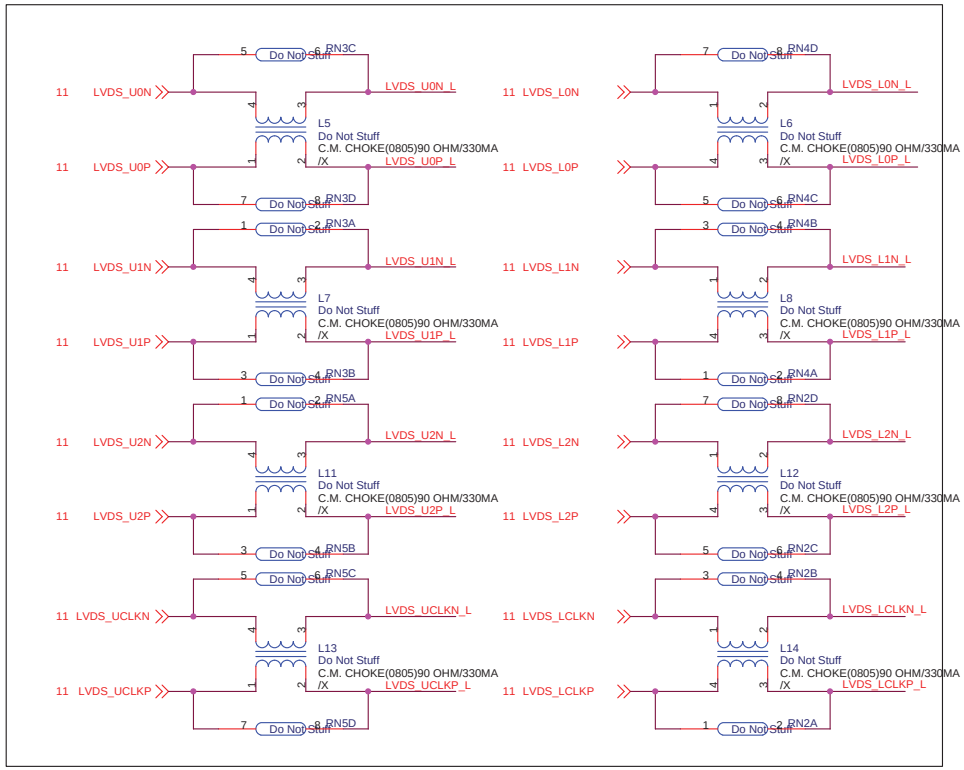
LUNCH

ASUSTek Computer INC.	Title : CRT Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 20 of 63	

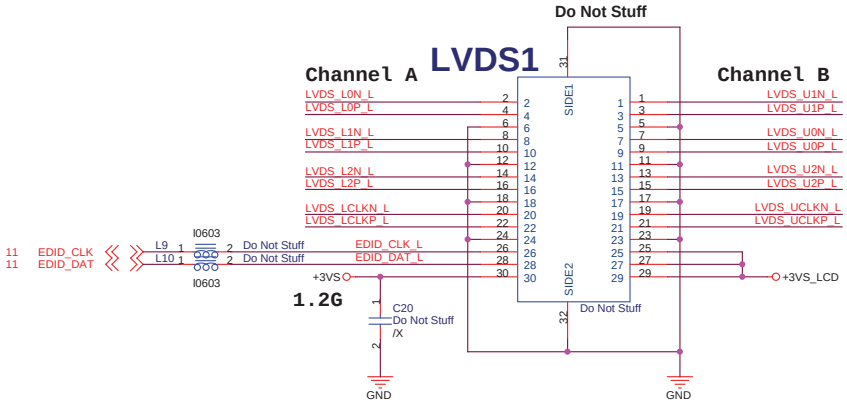
LCD Power Switch

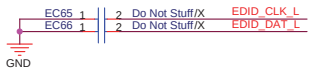






LVDS Connector





Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

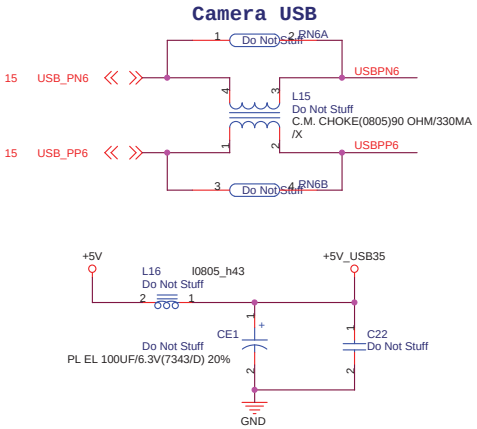
LUNCH

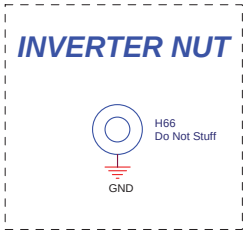
ASUSTek Computer INC.	Title : LVDS Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 21 of 63	

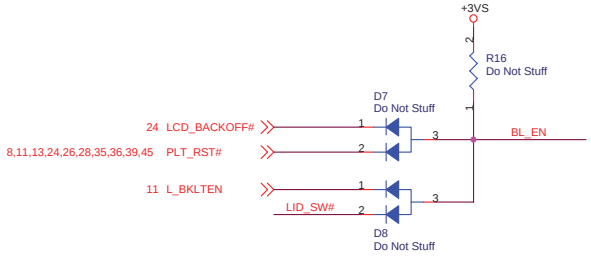
INVERTER Interface

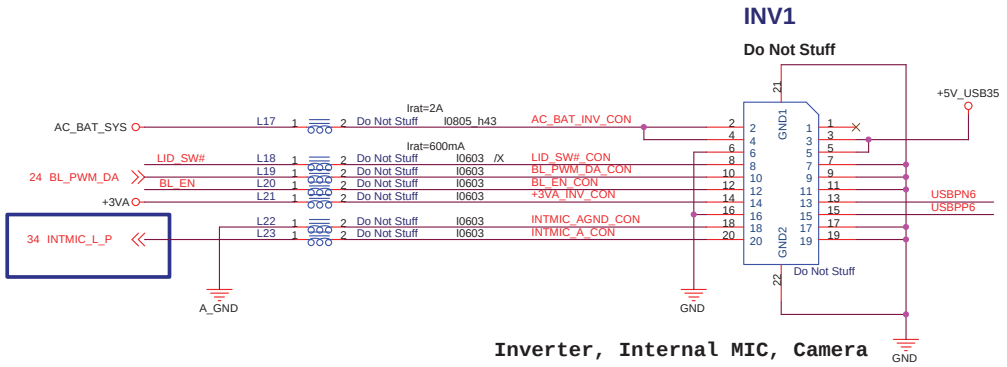
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back light.
Inverter Board built in 14.1W LCD Panel

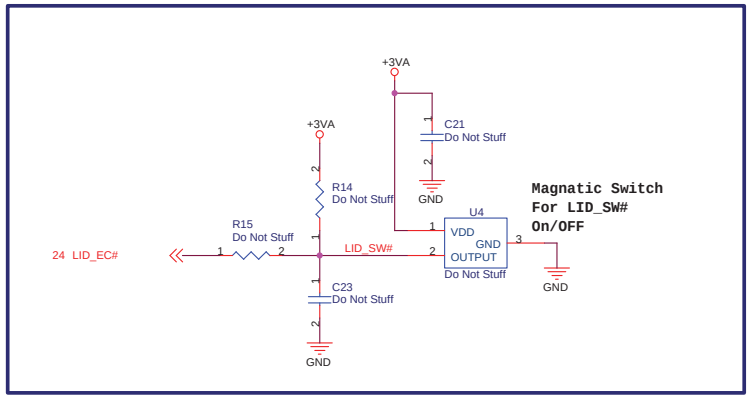


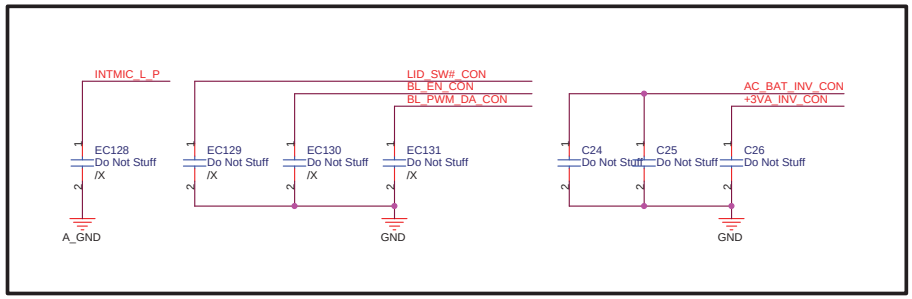






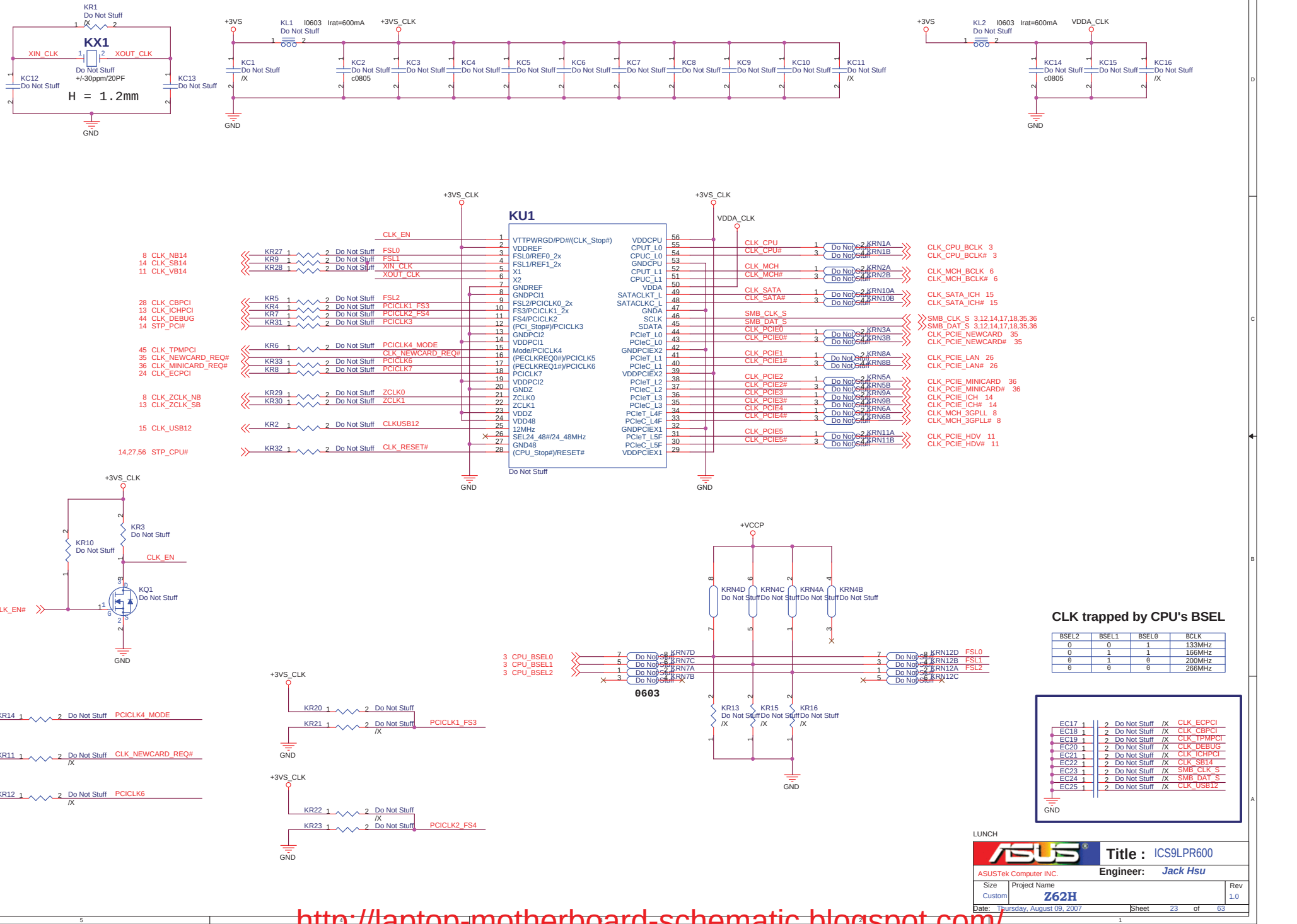
Inverter, Internal MIC, Camera





LUNCH

ASUSTek Computer INC.	Title : Inverter	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 22 of 63	



CLK trapped by CPU's BSEL

BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

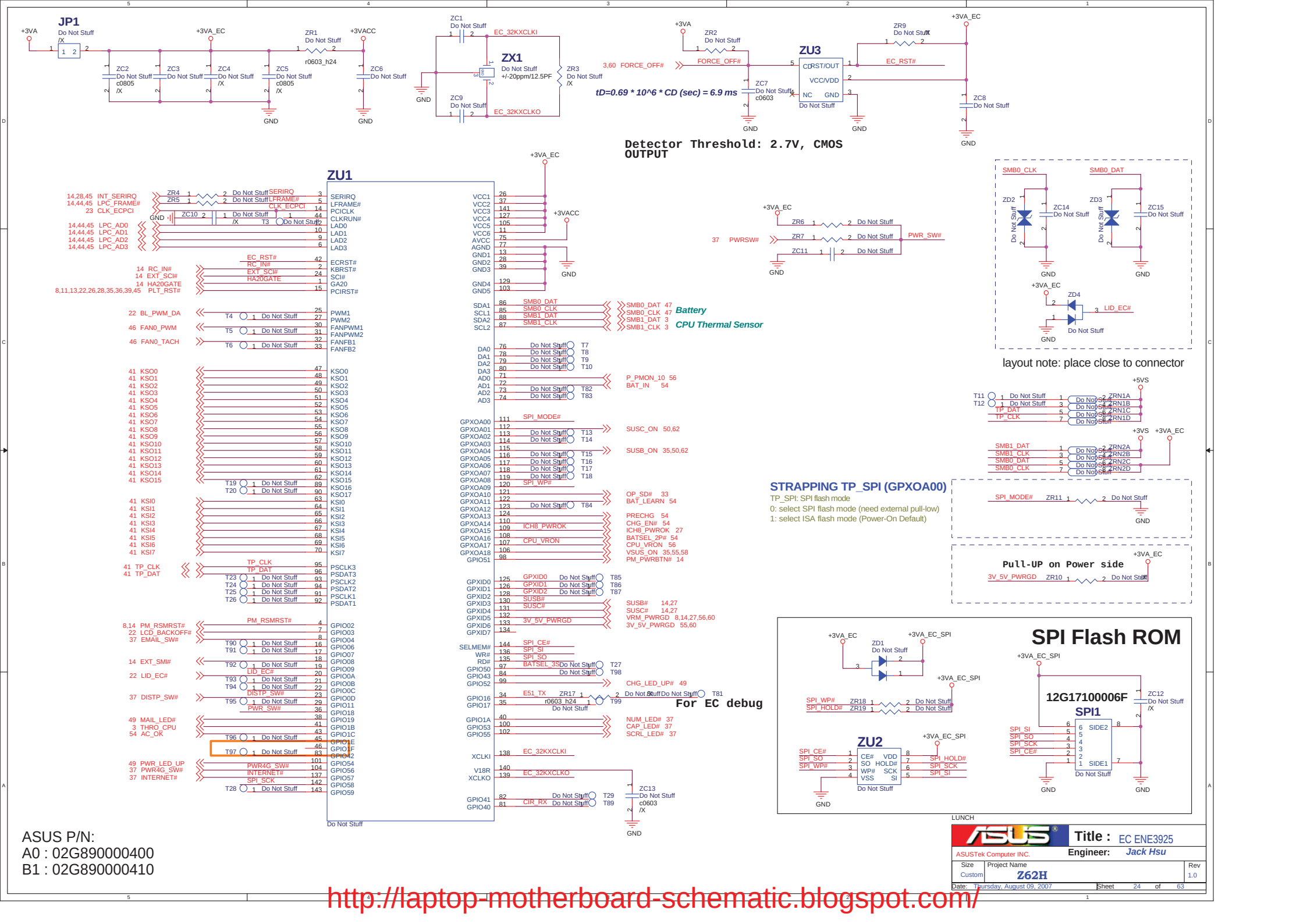
LUNCH

Title : ICS9LPR600

ASUSTek Computer INC. **Engineer:** *Jack Hsu*

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 23 of 63



ASUS P/N:
A0 : 02G890000400
B1 : 02G890000410

LUNCH

ASUSTek Computer INC.	Title : BLANK	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 25 of 63	

ASUS P/N:
A2:02G751006700
B0:02G751006710

+1.2VSUS_LAN **290mA**

T1C4 Do Not Stuff
T1C5 Do Not Stuff
T1C6 Do Not Stuff /X
T1C7 Do Not Stuff /X
GND

+1.8VSUS_LAN **150mA**

T1C8 Do Not Stuff
T1C9 Do Not Stuff
T1C10 Do Not Stuff /X
T1C11 Do Not Stuff /X
T1C12 Do Not Stuff /X
GND

+3VSUS **80mA**

T1C13 Do Not Stuff /X
T1C14 Do Not Stuff /X
T1C15 Do Not Stuff /X
T1C29 Do Not Stuff c0805
T1C30 Do Not Stuff c0805
GND

+3VS
T1C3 Do Not Stuff /X
GND

T1R1 Do Not Stuff /X
T1X1 Do Not Stuff
T1_XTALIN
T1_XTALOUT
T1C16 Do Not Stuff
T1C17 Do Not Stuff
GND

T1U2
A0 A1 A2 GND VCC WP SCL SDA
Do Not Stuff
+3VSUS
LAN_EECLK
LAN_EEDATA
GND

T1U1 Do Not Stuff

+1.2VSUS_LAN
+3VSUS
+3VS
LAN_EEDATA
LAN_EECLK
GND

VDD7 VMAIN_AVBL TESTMODE VDDO_TTL3 VDD6 Reserved4 CLKREQn VPD_DATA VDDO_TTL2 VDD5 VPD_CLK SPI_CLK SPI_CS SPI_DI SPI_DO VDD4

8 PCIE_RXP2_LAN
8 PCIE_RXN2_LAN
T1C2 Do Not Stuff
T1C1 Do Not Stuff
PCIE_RXP2_LAN_C
PCIE_RXN2_LAN_C
8 PCIE_TXN2_LAN
8 PCIE_TXP2_LAN
23 CLK_PCIE_LAN
23 CLK_PCIE_LAN#
PCIE_TXN2_LAN
PCIE_TXP2_LAN
+1.2VSUS_LAN
+3VSUS

49 TX_P
50 TX_N
51 NC2
52 NC3
53 RX_N
54 RX_P
55 REFCLKP
56 REFCLKN
57 NC4
58 VDD8
59 LED_ACTn
60 LED_LINK10/100n
61 VDDO_TTL4
62 LED_LINK1000n
63 LED_DUPLEXn
64 NC5
65 GND

+1.8VSUS_LAN

32 NC1
31 MDIN[3]
30 MDIP[3]
29 Reserved3
28 AVDD4
27 MDIN[2]
26 MDIP[2]
25 Reserved2
24 Reserved1
23 AVDD3
22 AVDD2
21 MDIN[1]
20 MDIP[1]
19 AVDD1
18 MDIN[0]
17 MDIP[0]

MDIN3 40
MDIP3 40
MDIN2 40
MDIP2 40
MDIN1 40
MDIP1 40
MDIN0 40
MDIP0 40

VDDO_TTL1 VDD1 CTRL12 CTRL18 PERSTn/TSTPT WAKEn VDD2 AVDDH(3.3V) SWITCH_VAUX LOM_DISABLEn SWITCH_VCC VAUX_AVLBL VDD3 XTALO XTALI RSET

+1.2VSUS_LAN +3VSUS

Keep at least 25mils trace width
LAN_+1.2VSUS_CTRL_25MIL
LAN_+1.8VSUS_CTRL_25MIL

8,11,13,22,24,28,35,36,39,45 PLT_RST#
8,15,35,36 PCIE_WAKE#

LAN_RSET
T1_XTALIN
T1_XTALOUT
8056_LAN_RST#

T1C18 Do Not Stuff
T1C19 Do Not Stuff
T1C20 Do Not Stuff
T1C21 Do Not Stuff
T1R4 Do Not Stuff 1%
T1R5 Do Not Stuff 1%
T1R6 Do Not Stuff 1%
T1R7 Do Not Stuff 1%
T1R8 Do Not Stuff 1%
T1R9 Do Not Stuff 1%
T1R10 Do Not Stuff 1%
T1R11 Do Not Stuff 1%
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
GND

*All termination resistors should be near chip

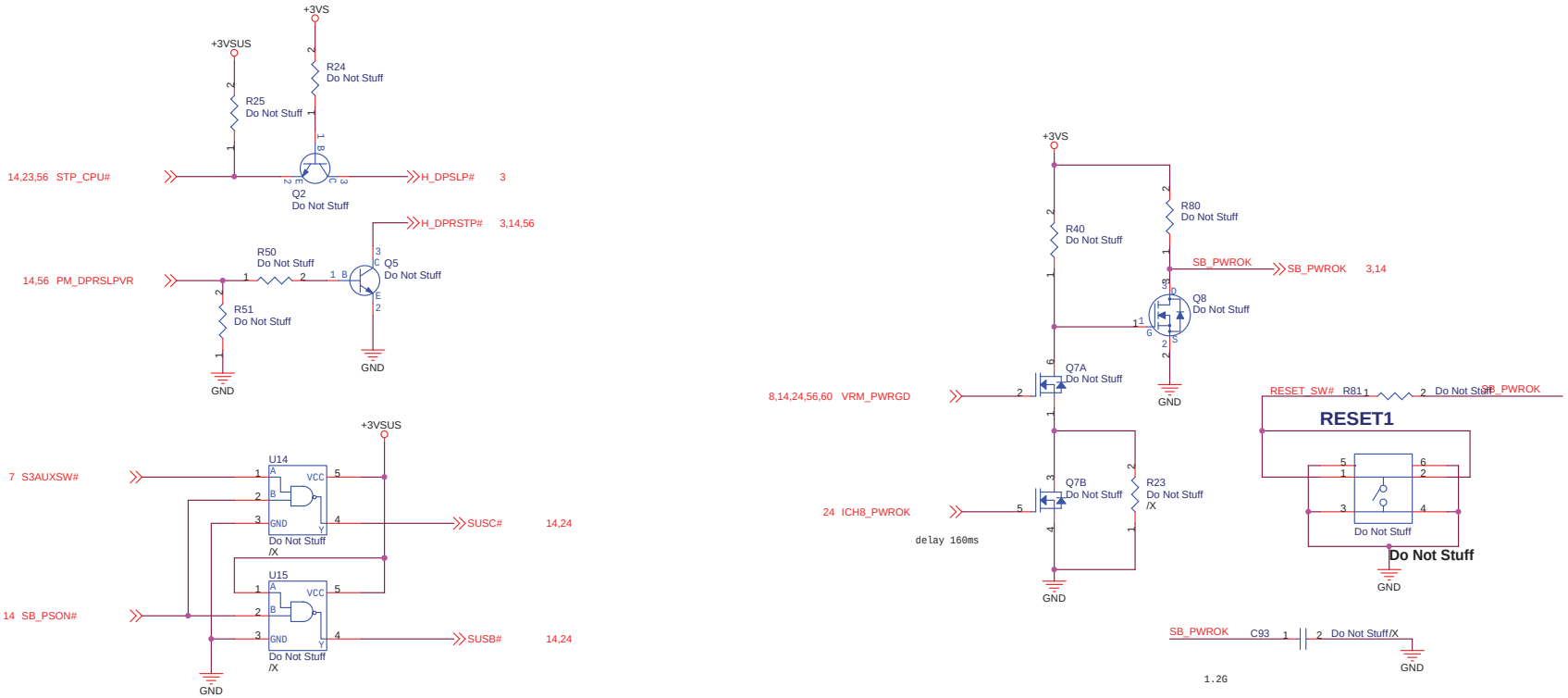
+3VSUS
LAN_RSET
T1R12 Do Not Stuff 1%
T1R13 Do Not Stuff
T1R2 Do Not Stuff
T1R3 Do Not Stuff
LAN_EEDATA
LAN_EECLK
8056_LAN_RST#
T1C28 Do Not Stuff c0402
GND

+3VSUS
LAN_+1.2VSUS_CTRL_25MIL
T1R16 Do Not Stuff
T1R17 Do Not Stuff
T1Q1 Do Not Stuff
T1C23 Do Not Stuff
T1C22 Do Not Stuff /X
T1C24 Do Not Stuff c0805
+1.2VSUS_LAN
GND
SHAPE

+3VSUS
LAN_+1.8VSUS_CTRL_25MIL
T1R18 Do Not Stuff
T1R19 Do Not Stuff
T1Q2 Do Not Stuff
T1C26 Do Not Stuff
T1C25 Do Not Stuff /X
T1C27 Do Not Stuff c0805
+1.8VSUS_LAN
GND
SHAPE

LUNCH

ASUSTek Computer INC.	Title : LAN Marvell 88E8056	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Monday, August 13, 2007	Sheet 26 of 63	



Power ON & OFF:

	S5 → S0 → S5		
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC#(S4)	0	1	0
SUSB#(S3)	0	1	0
Power Status	System	Main	System

Sleep & Wake up

	S0 → S3 → S0				
S3AUXSW#	1	0	0	0	1
SB_PSON#	0	0	1	0	0
SUSC#(S4)	1	1	1	1	1
SUSB#(S3)	1	1	0	1	1
Power Status	Main	Main	System, S4	Main	Main

LUNCH

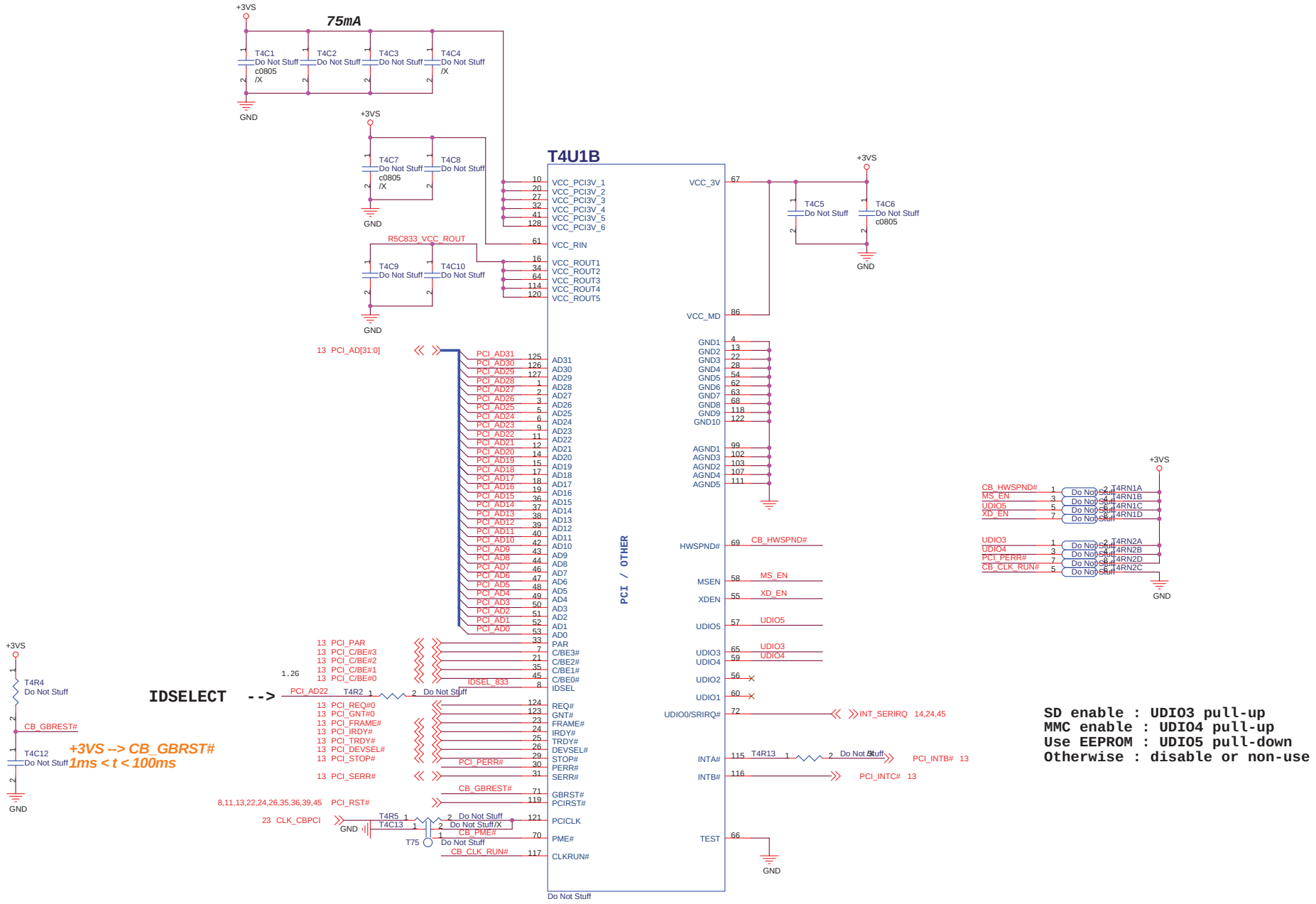
ASUSTek Computer INC.

Title : OTHER

Engineer: Jack Hsu

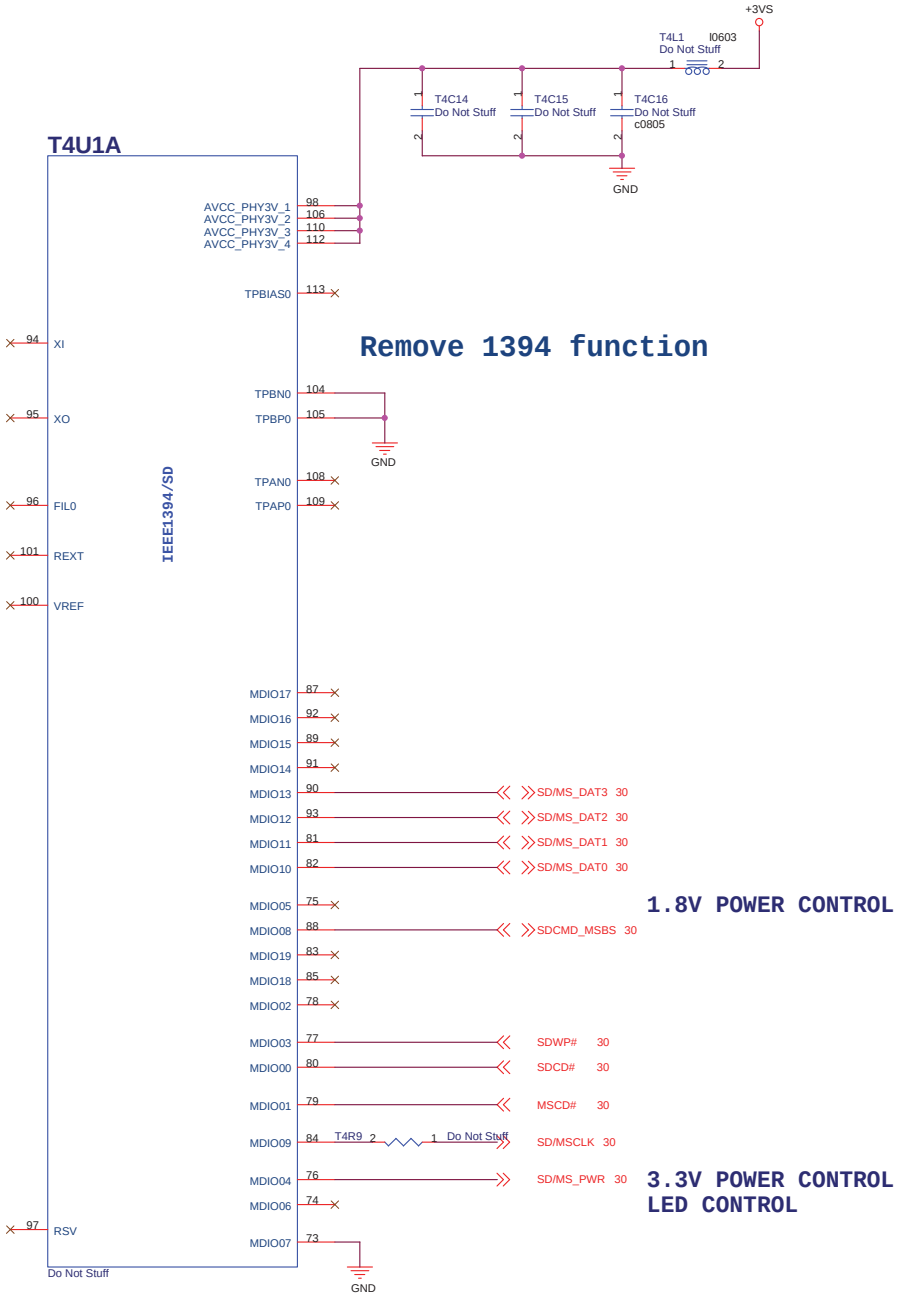
Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 27 of 63



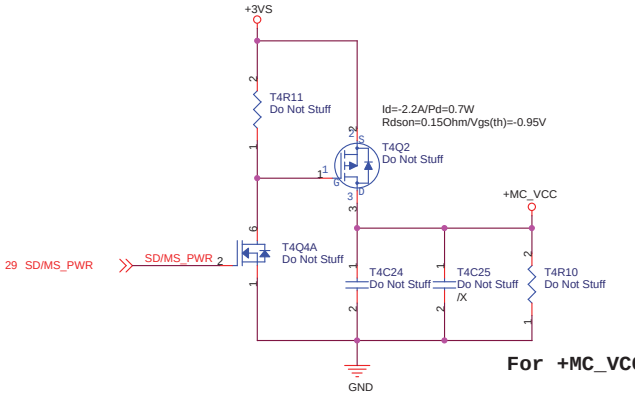
LUNCH

ASUSTek Computer INC.	Title : R5C833_PCI	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 28 of 63	



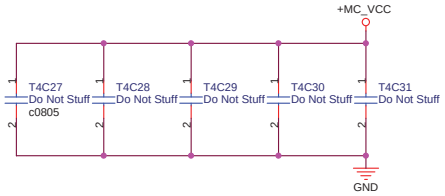
LUNCH

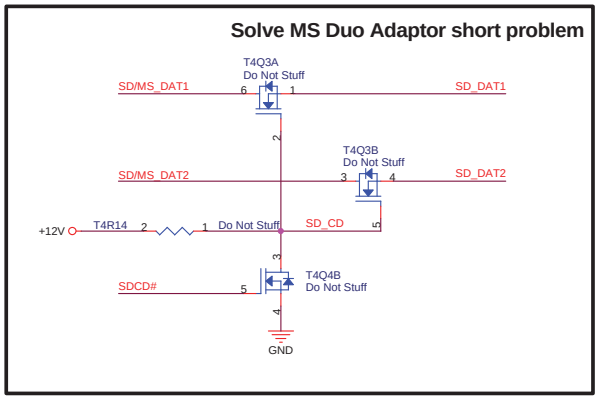
ASUSTek Computer INC.	Title : R5C833_1394/SD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 29 of 63	

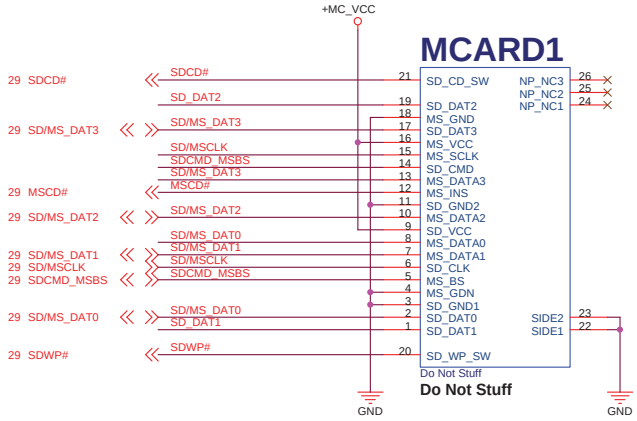


For +MC_VCC discharg

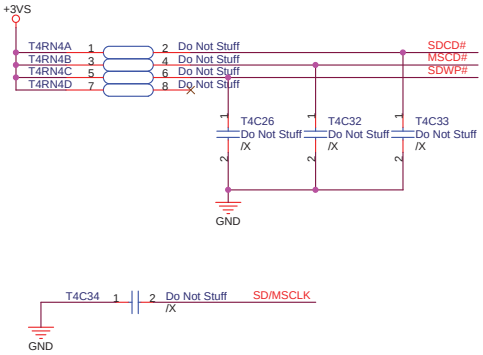
Card Reader Power Switcher





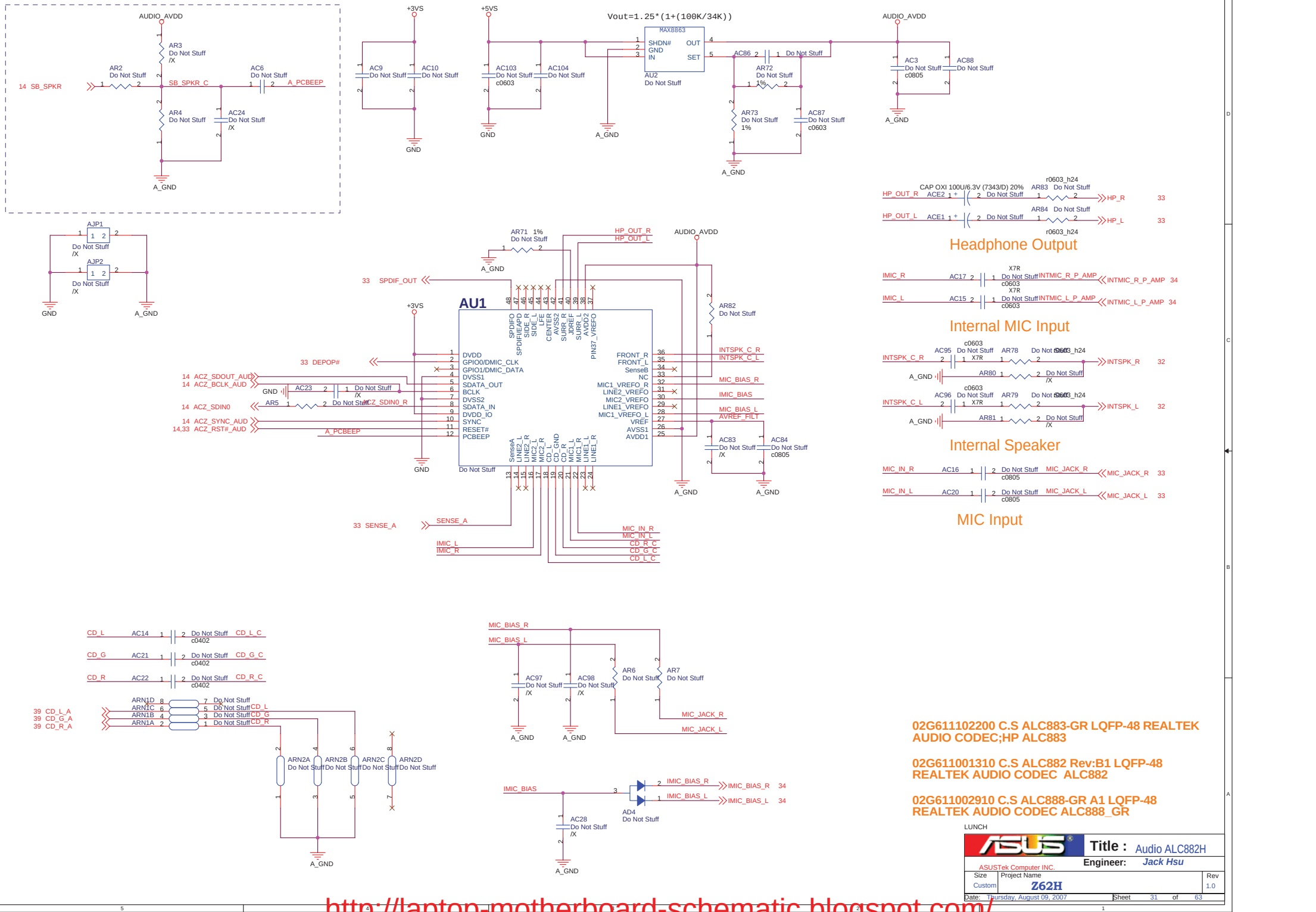


3 in 1 Card Reader



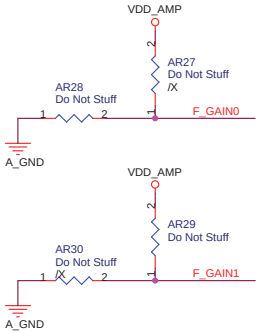
LUNCH

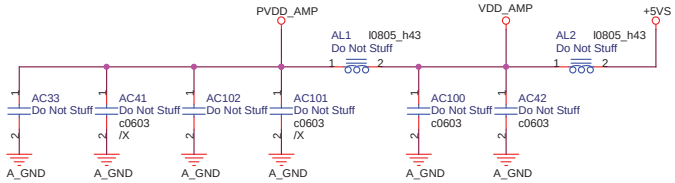
ASUSTek Computer INC.	Title: 3 in 1 Card Reader	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 30 of 63	

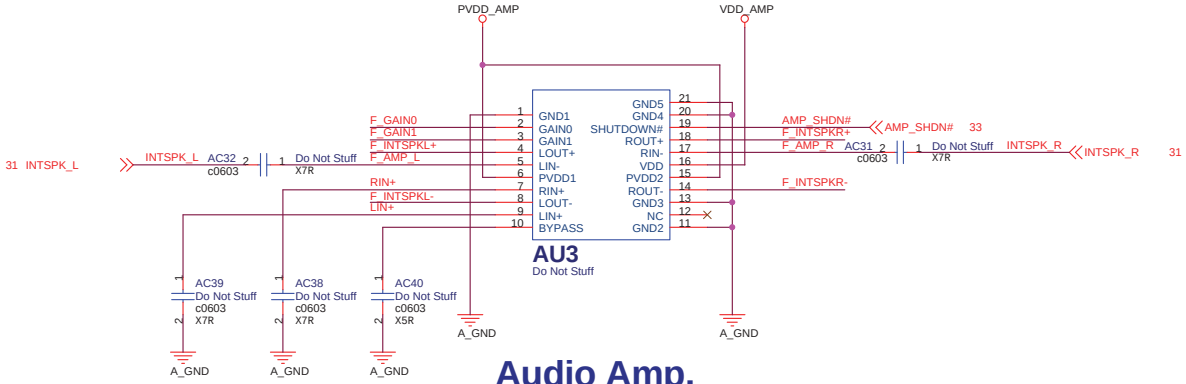


GAIN Control

GAIN0	GAIN1	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db

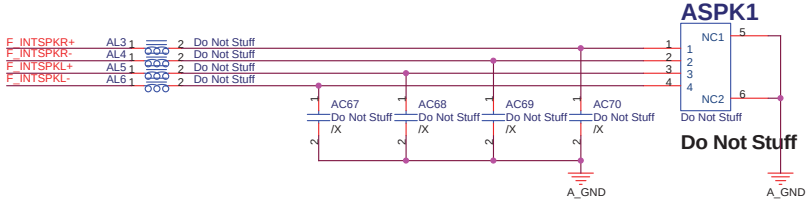






Audio Amp.
fc = 1kHz

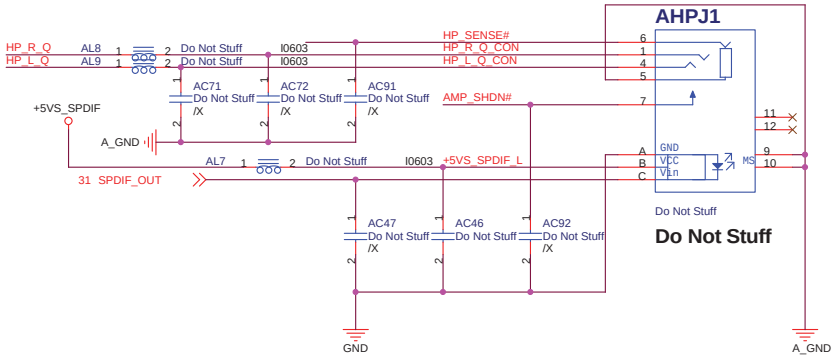
12G171000047
Internal Speaker Connector

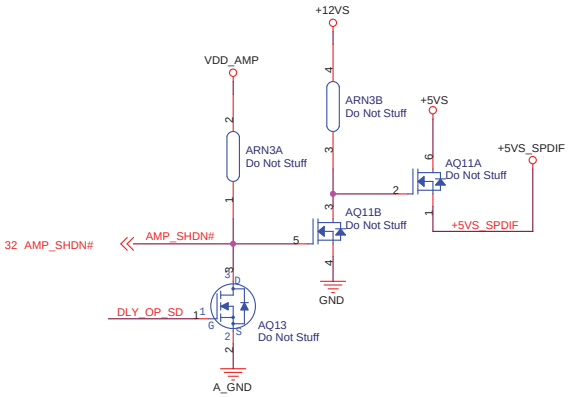


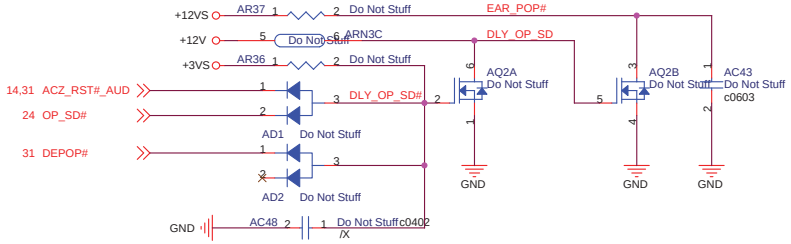
LUNCH

ASUSTek Computer INC.	Title : Audio Amp. & Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 32 of 63	

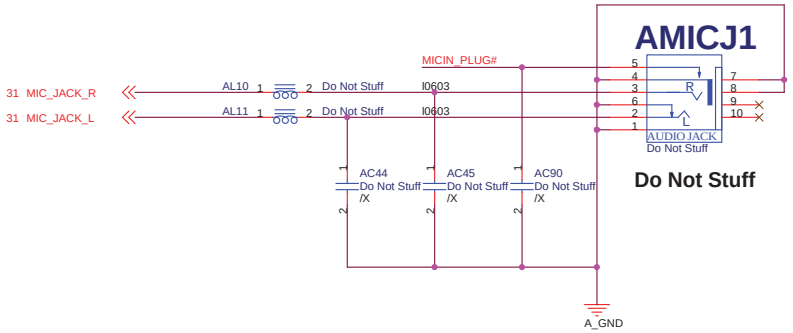
Headphone & S/PDIF Jack







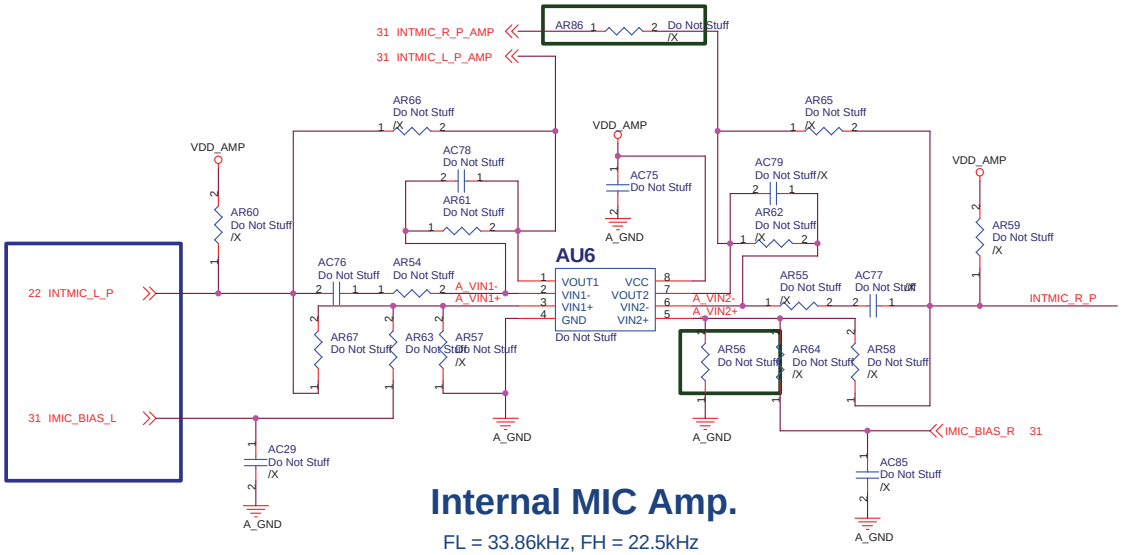
Microphone-In Jack



Jack Plug-in Detection

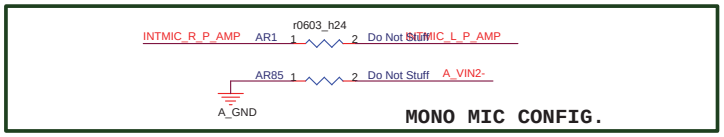
LUNCH

ASUSTek Computer INC.	Title : Audio JACK	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 33 of 63	



Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz



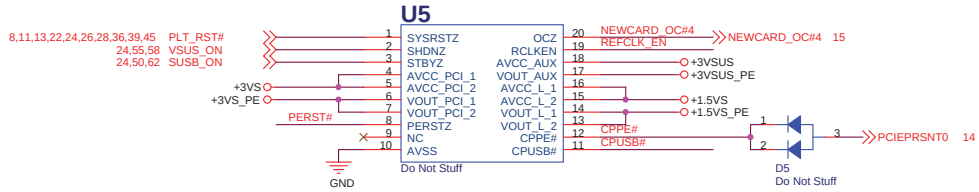
LUNCH

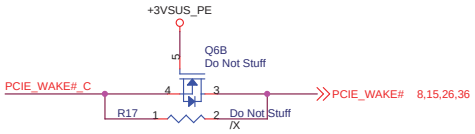
ASUSTek Computer INC.	Title : MIC PreAmp.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 34 of 63	

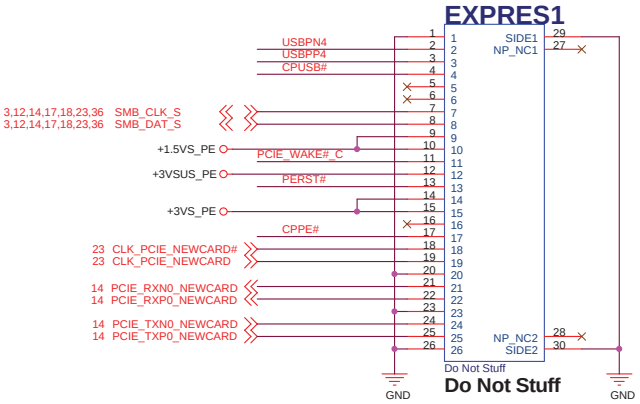
06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1

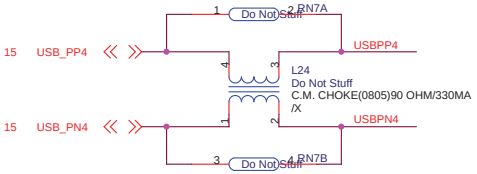
06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

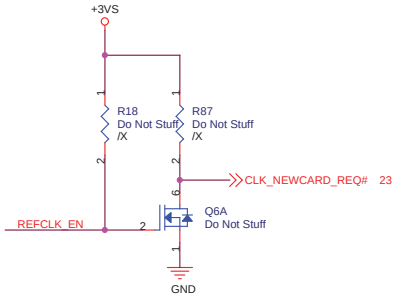
NewCard Header





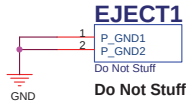


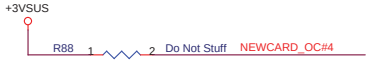


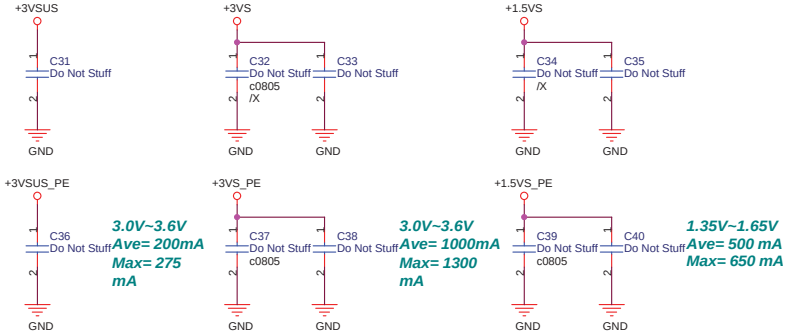


ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector

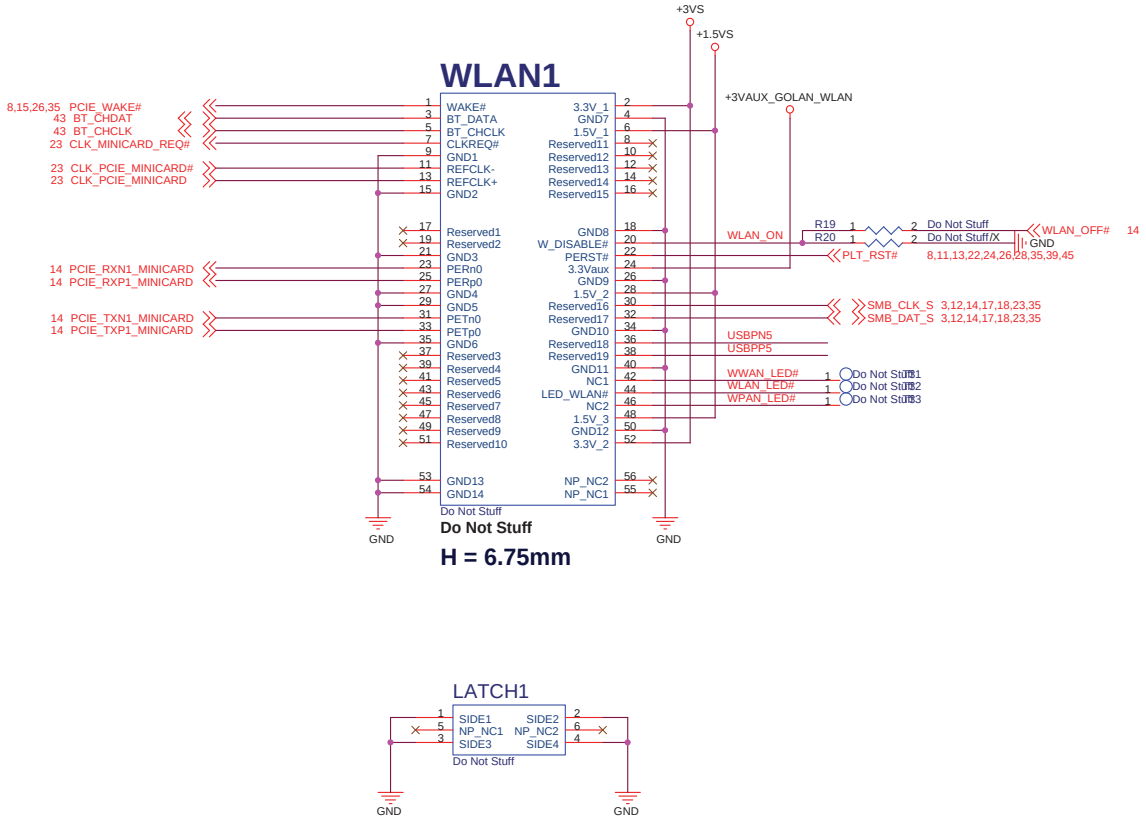


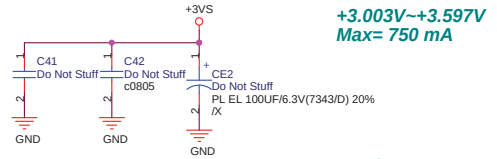




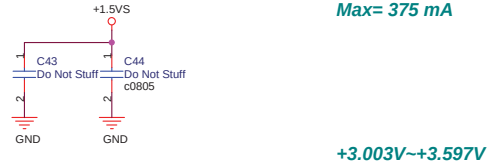
LUNCH

ASUSTek Computer INC.	Title : NEWCARD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 35 of 63	

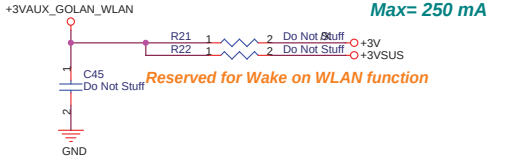




+3.003V~+3.597V
Max= 750 mA

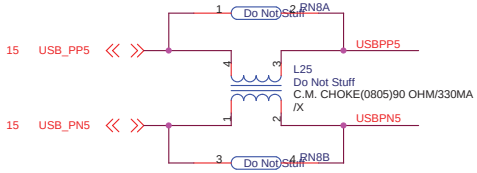


+1.425V~+1.575V
Max= 375 mA



+3.003V~+3.597V
Max= 250 mA

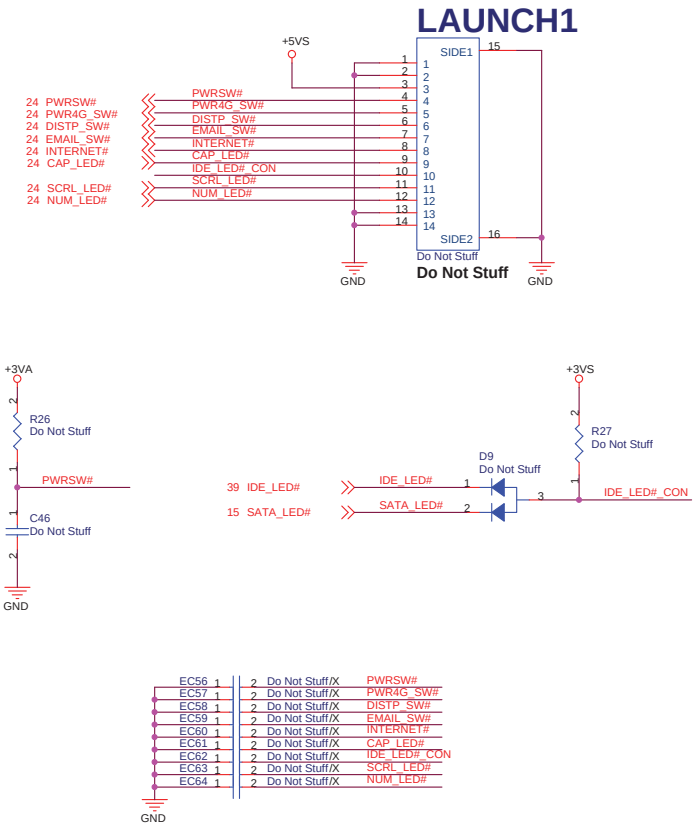
Reserved for Wake on WLAN function



LUNCH

ASUSTek Computer INC.	Title : MINICARD - WLAN	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 36 of 63	

LAUNCH BOARD Connector



LUNCH

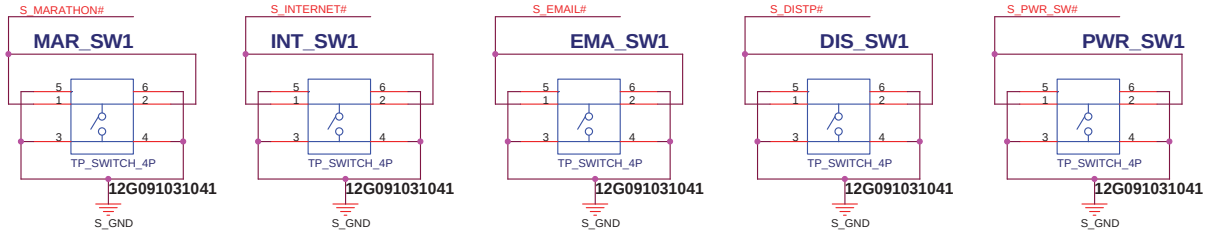
Title : LAUNCH_B Conn.

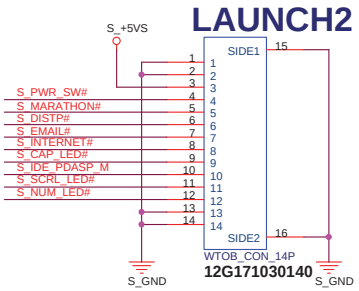
ASUSTek Computer INC.

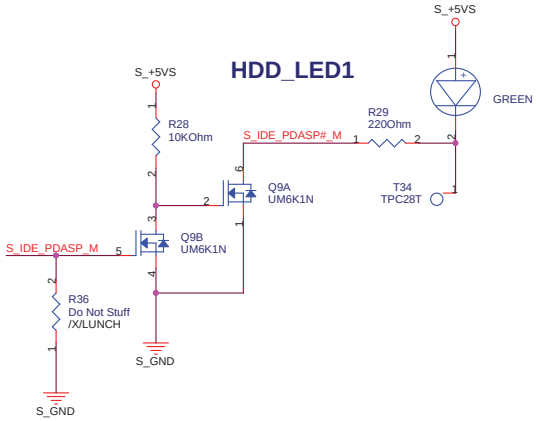
Engineer: Jack Hsu

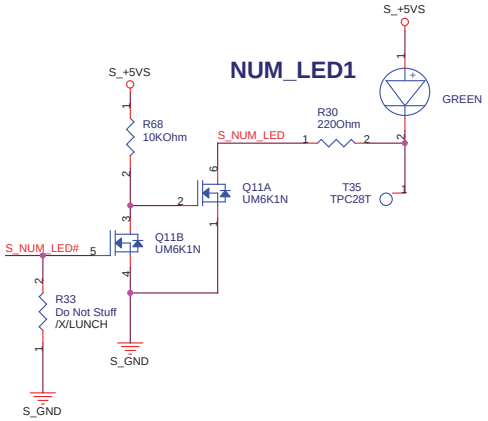
Size	Project Name	Rev
Custom	Z62H	1.0

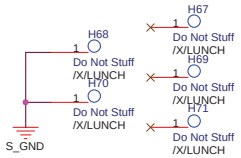
Date: Thursday, August 09, 2007 Sheet 37 of 63

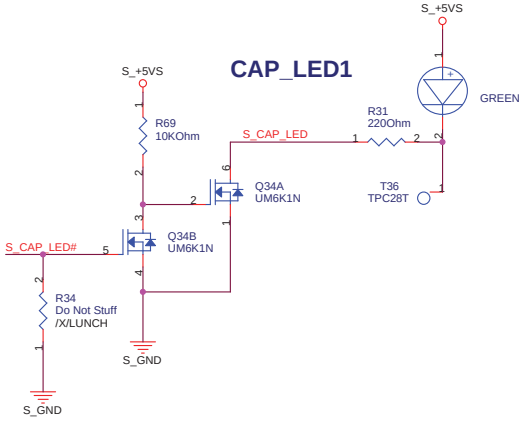


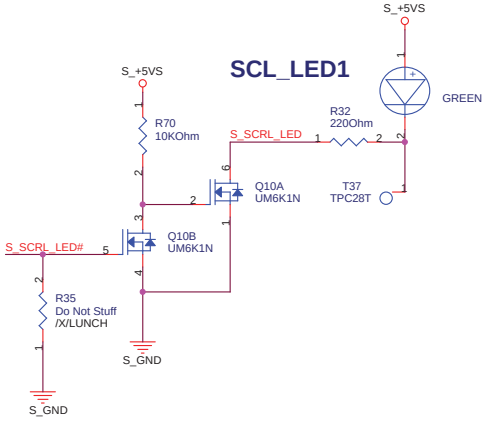












LUNCH

ASUSTek Computer INC.

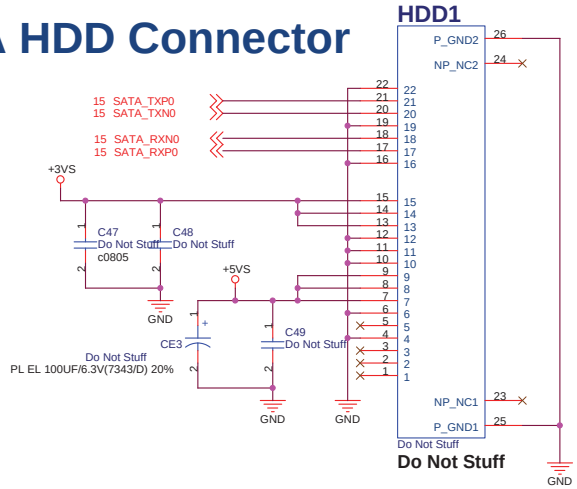
Title : LAUNCH BOARD

Engineer: Jack Hsu

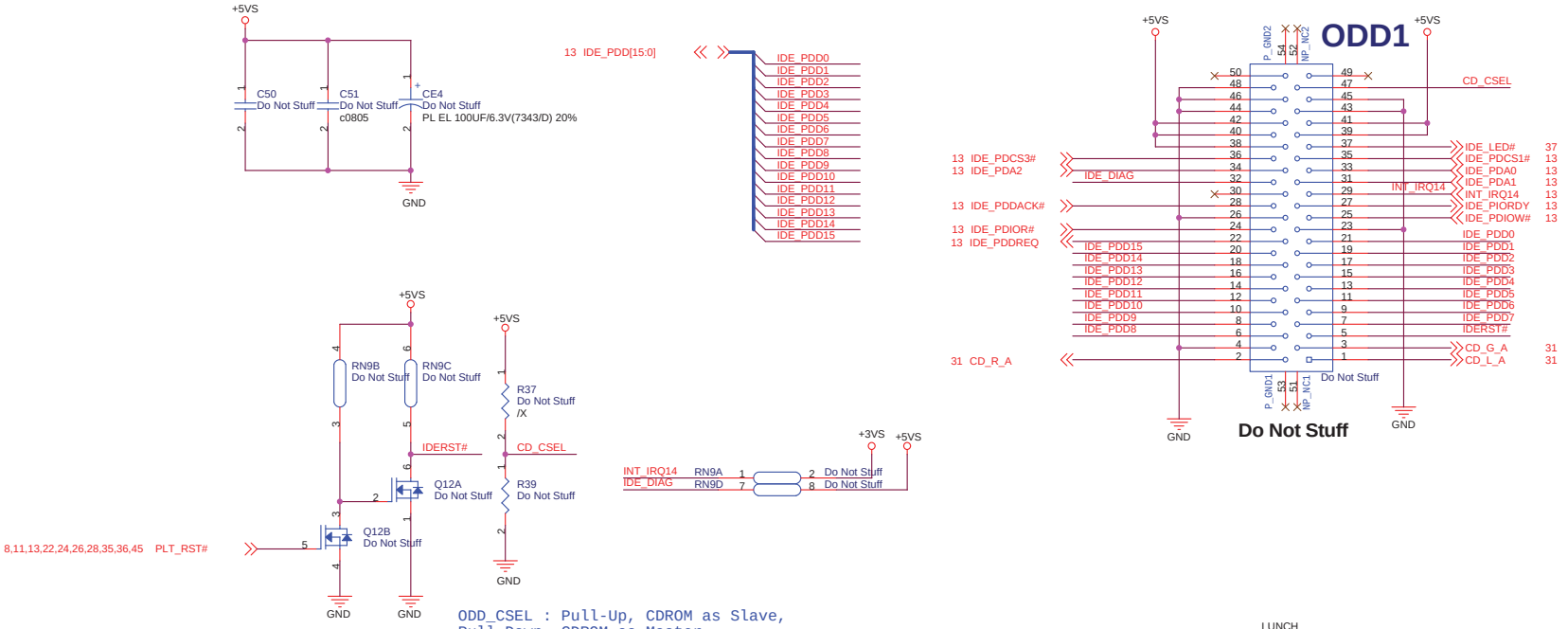
Size	Project Name	Rev
Custom	Z62H	1.0

Date: Monday, August 13, 2007 Sheet 38 of 63

SATA HDD Connector



ODD Connector

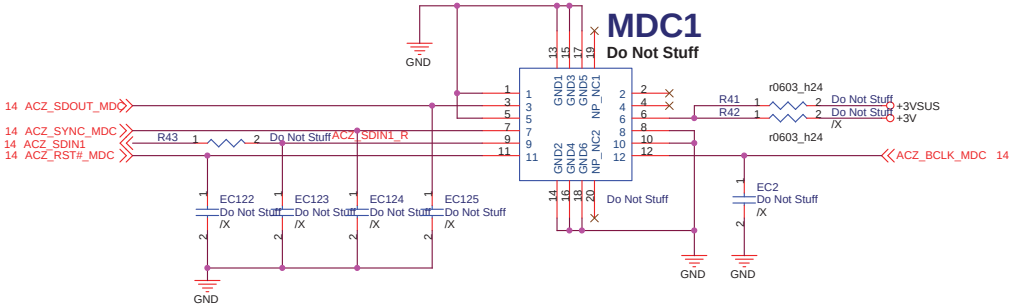


ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master

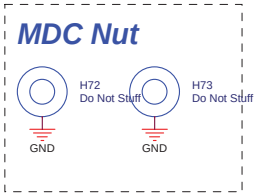
LUNCH

ASUSTek Computer INC.	Title : HDD & ODD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 39 of 63	

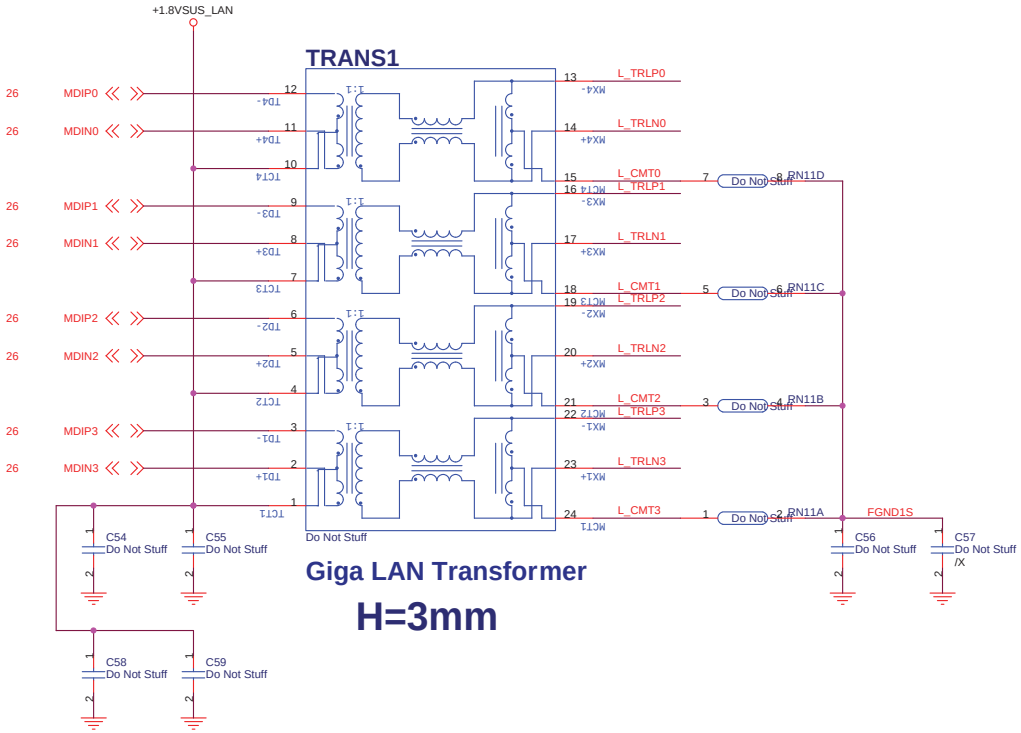
MDC Connector



MDC Nut

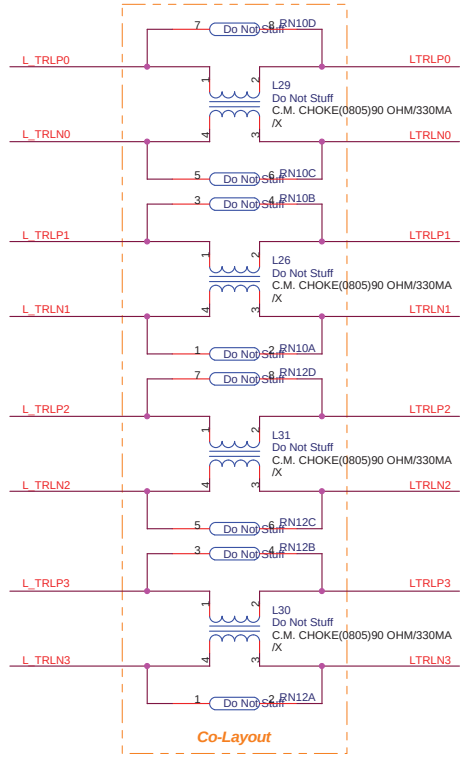


TRANS1

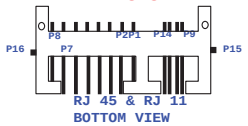


Giga LAN Transformer

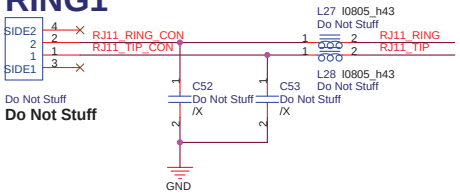
H=3mm



12-142313122

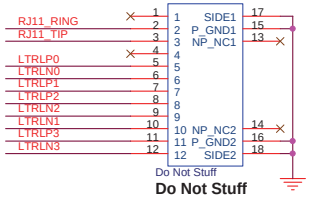


RING1



Do Not Stuff

RJ45_11

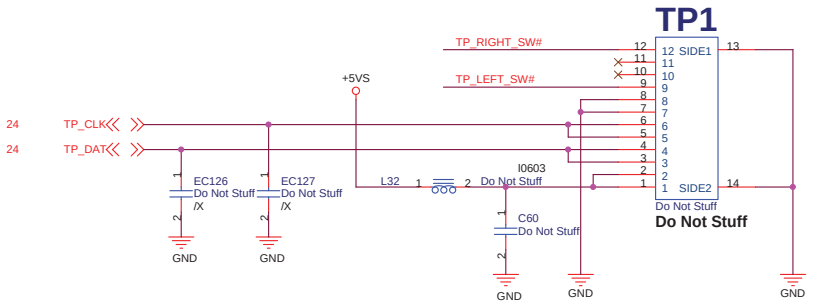


Do Not Stuff

LUNCH

ASUSTek Computer INC.	Title : MDC_RJ45_RJ11	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 40 of 63	

TouchPad Connector

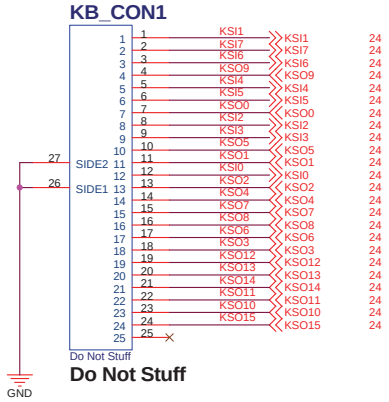


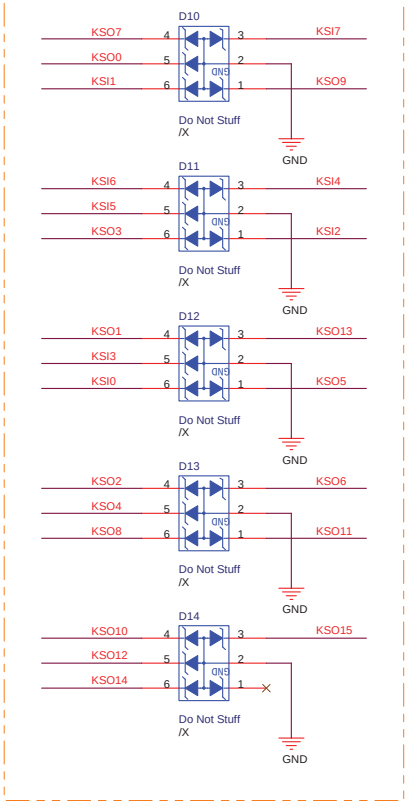
Touch pad Definition

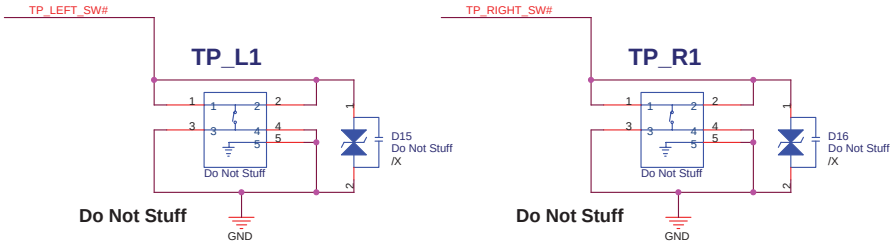
1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

Z62F: pin1 reversal

Keyboard Connector





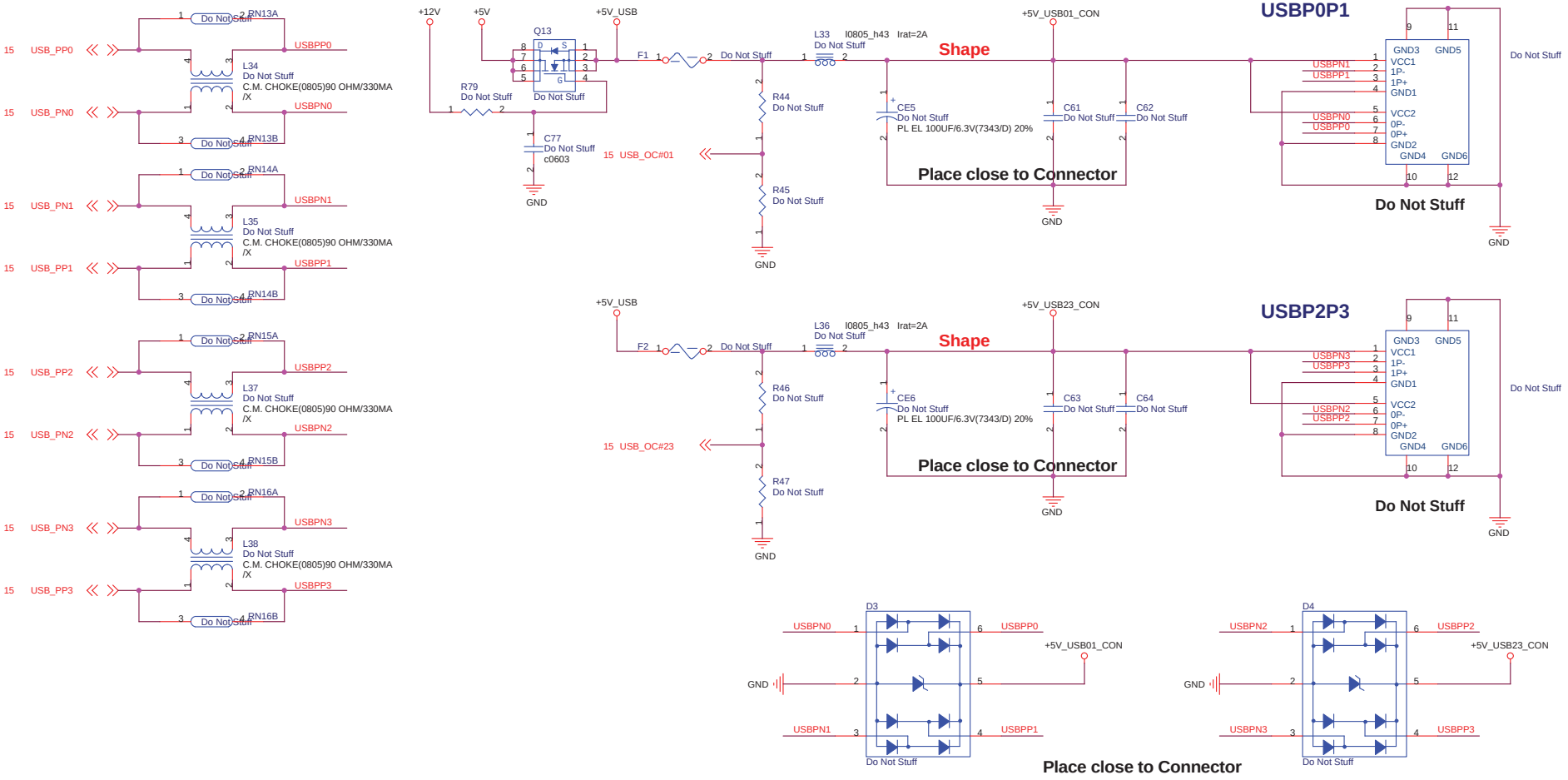


TOUCH PAD SWITCH

LUNCH

ASUSTek Computer INC.	Title : TP / KB Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 41 of 63	

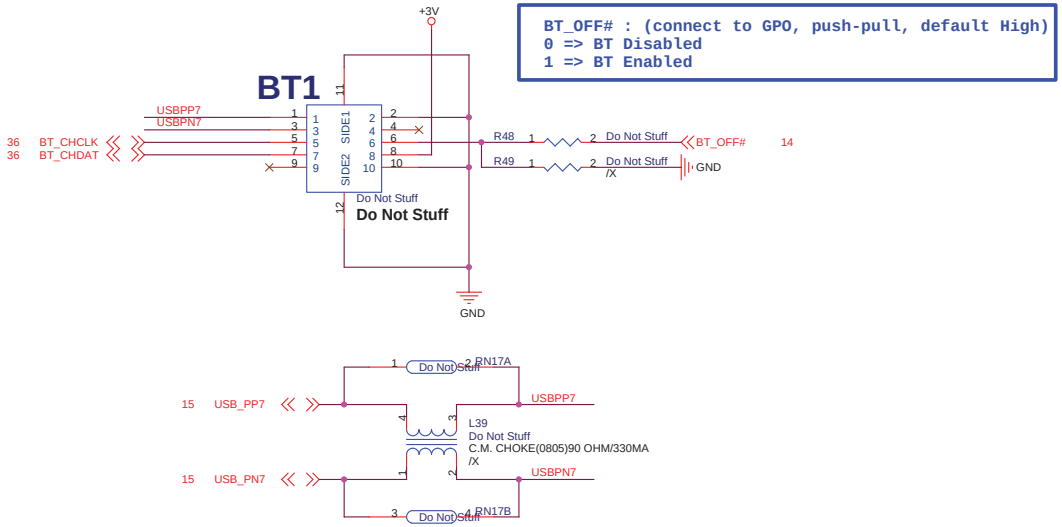
USB Power & OC Alert



LUNCH

ASUSTek Computer INC.	Title : USB Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 42 of 63	

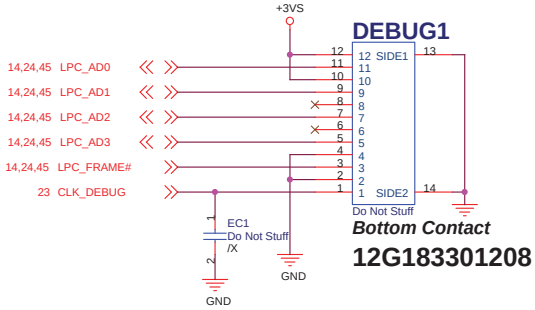
Bluetooth Connector



LUNCH

ASUSTek Computer INC.	Title : Bluetooth Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 43 of 63	

Debug Connector



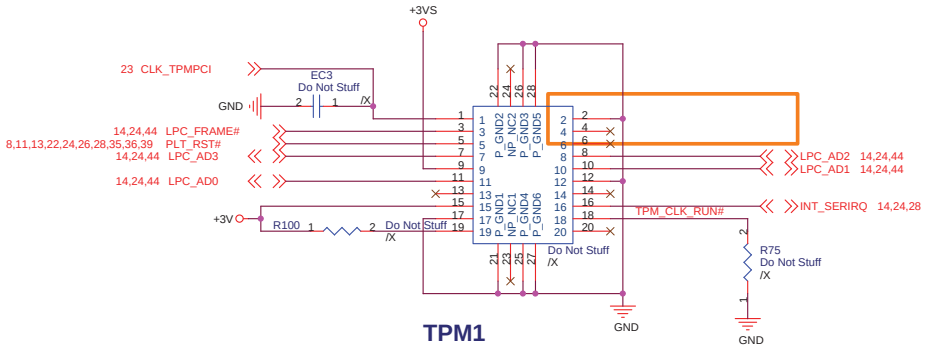
Bottom Contact

12G183301208

LUNCH

ASUSTek Computer INC.	Title : Debug Port	
	Engineer: *Jack Hsu*	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 44 of 63	

TPM Connector



TPM1

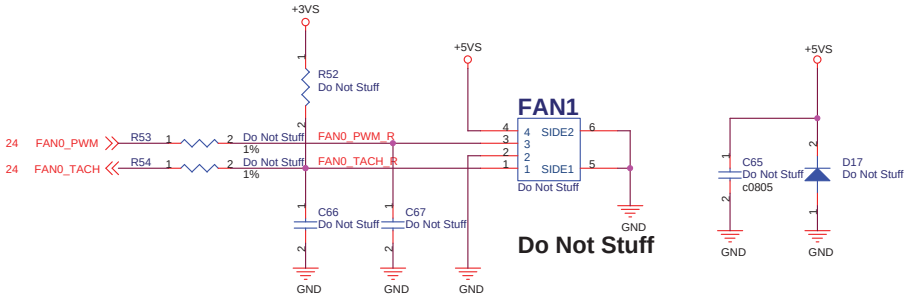
12G16080020J

Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
Removed!!

TPM Nut

LUNCH

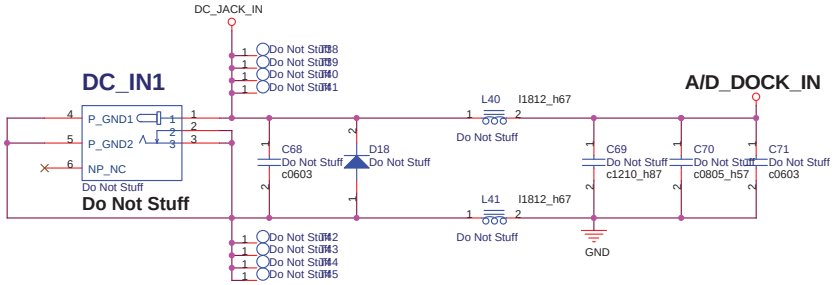
ASUSTek Computer INC.	Title : TPM Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 45 of 63	

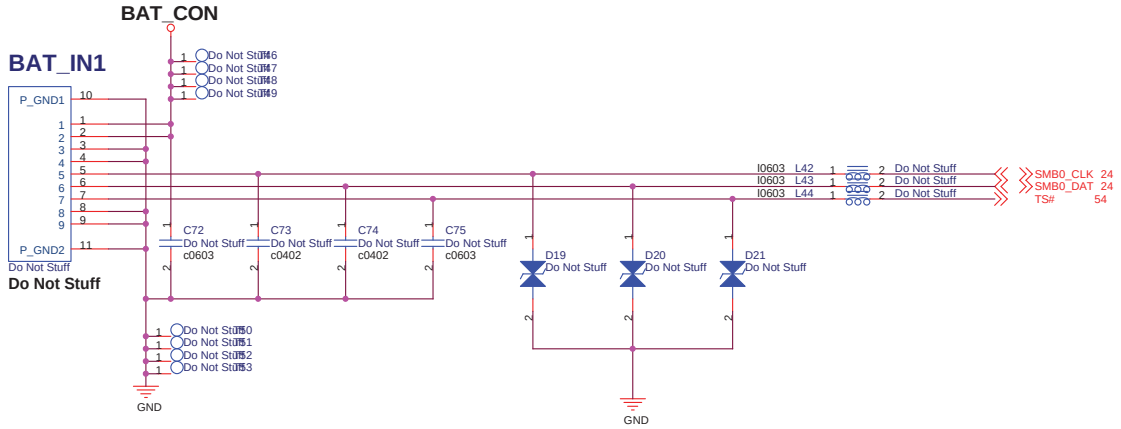


SYSTEM Fan Connector

LUNCH

ASUSTek Computer INC.	Title : Fan Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 46 of 63	





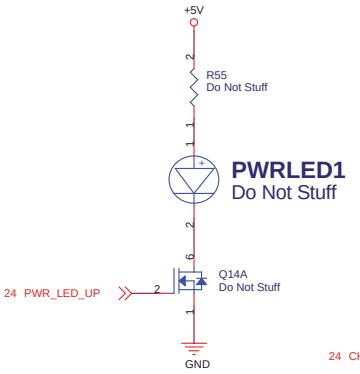
LUNCH

ASUSTek Computer INC.	Title : DC-IN & BAT-IN	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 47 of 63	

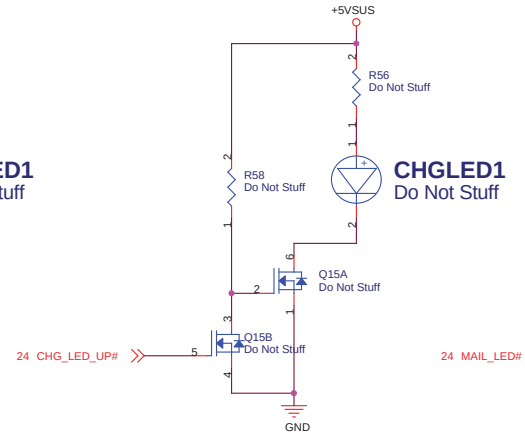
LUNCH

ASUSTek Computer INC.	Title : BLANK	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 48 of 63	

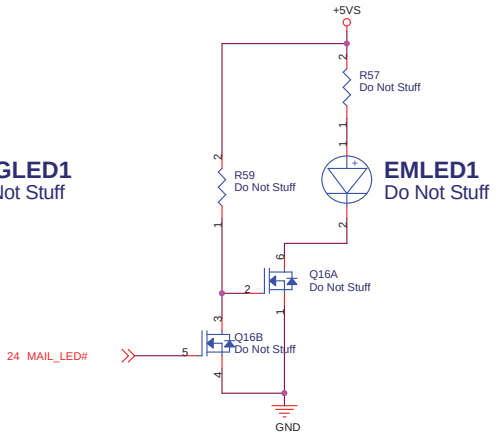
POWER LED



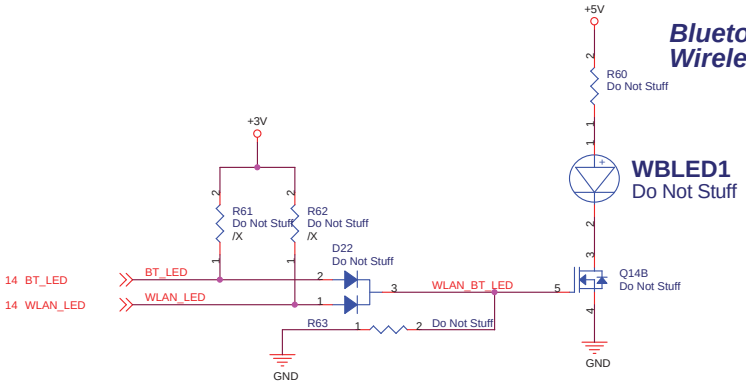
Battery Charge LED



Email LED

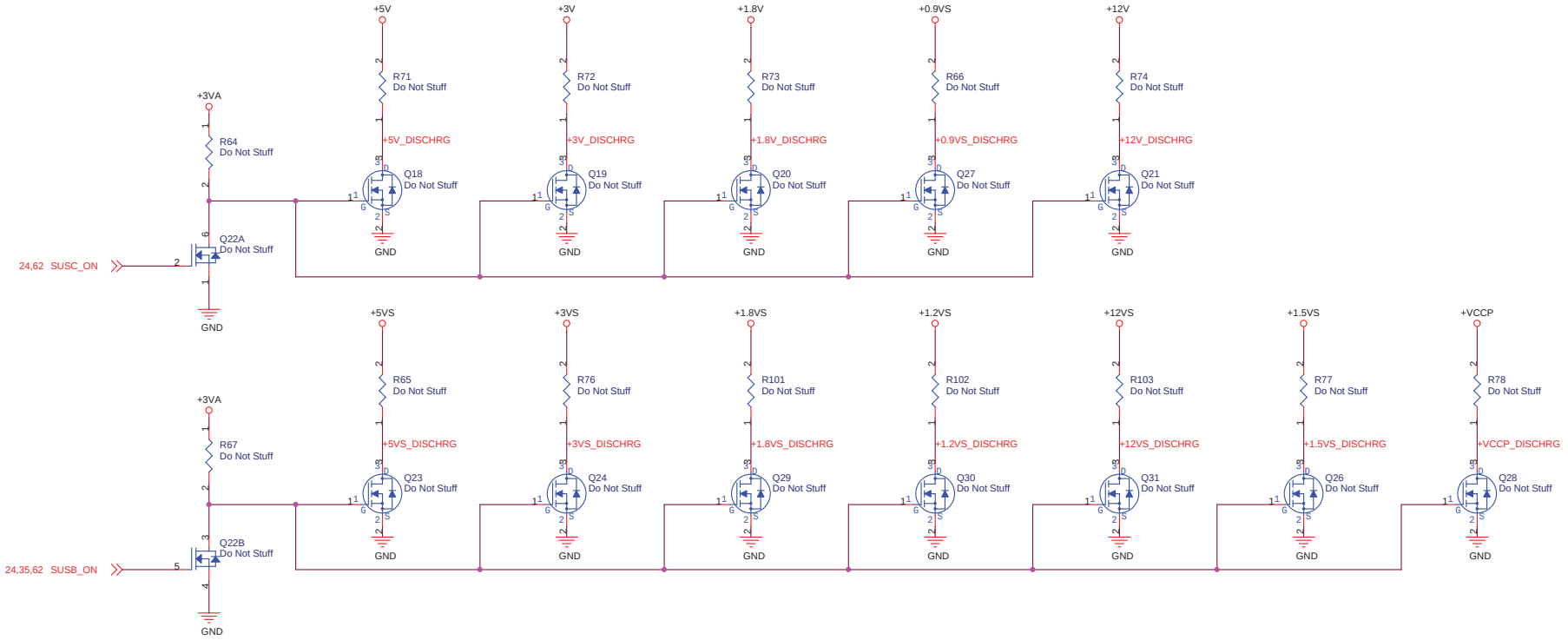


Bluetooth LED
Wireless LED



LUNCH

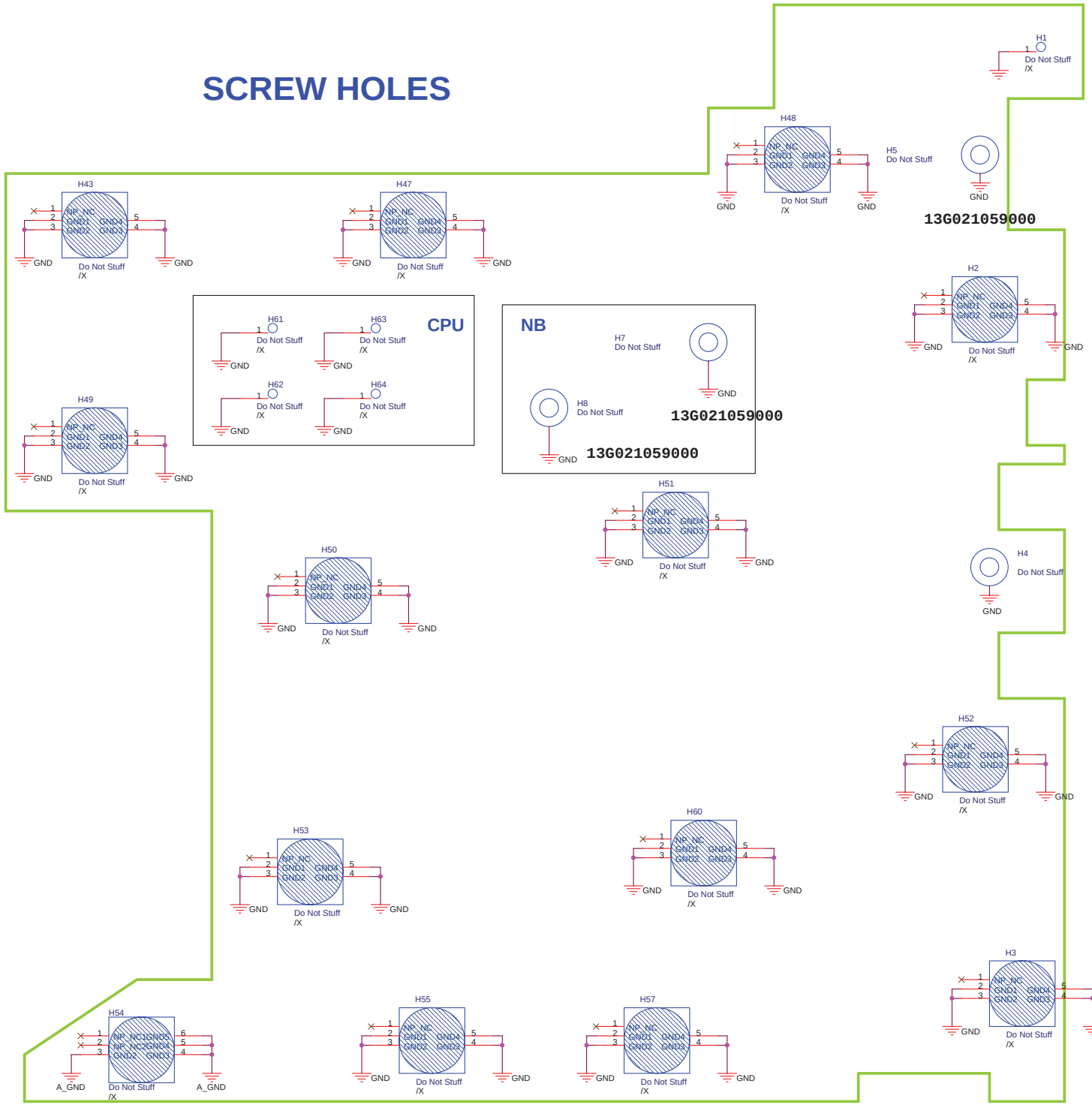
ASUSTek Computer INC.	Title : LED	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 49 of 63	



LUNCH

ASUSTek Computer INC.	Title : Discharger	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 50 of 63	

SCREW HOLES



Spring For EMI

136021034020	EPAD1	EPAD2	EPAD3	EPAD4	EPAD10
136021034030	EPAD5	EPAD6	EPAD7	EPAD8	EPAD9

Do Not Stuff
/X
N/A

LUNCH

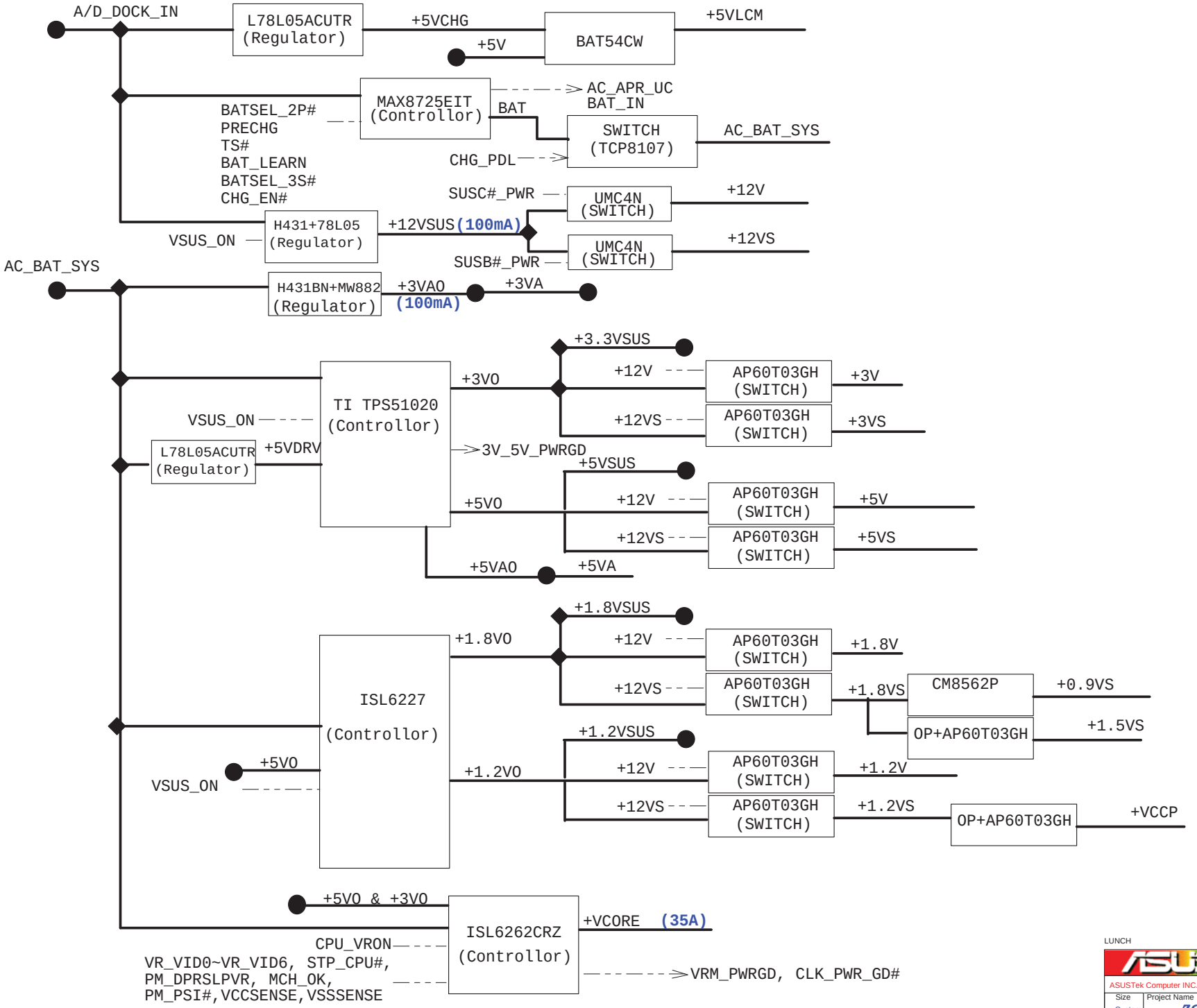
ASUSTek Computer INC.

Title : EMI CAP

Engineer: Jack Hsu

Size	Project Name	Rev
C	Z62H	1.0

Date: Friday, August 10, 2007 Sheet 52 of 63



LUNCH

ASUSTek Computer INC.

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 53 of 63

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

Adaptor Max. Current :

PR5708=20K PR5714 = 178K; Ilimit = 4.5A; 81W

PR5708=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

Victl = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V

=> Icharge = 2.9329A

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

BATSEL_2P# = 1, 3 Cells

BATSEL_2P# = 0, 6 or 9 Cells

PRECHG = 1, Pre-Charging Mode

Charging Current = 156mA

CHG_EN# = 1, Charger Disabled

CHG_EN# = 0, Charger Enabled

AC_OK = 1, Adaptor is present

AC_OK = 0, Adaptor is absent

BAT_LEARN = 1, Battery discharges

BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

BAT_IN_OC# = 1; Battery absence

BAT_IN_OC# = 0; Battery Plug-in

TS# = 1; Battery absence

TS# = 0; Battery Plug-in

LUNCH

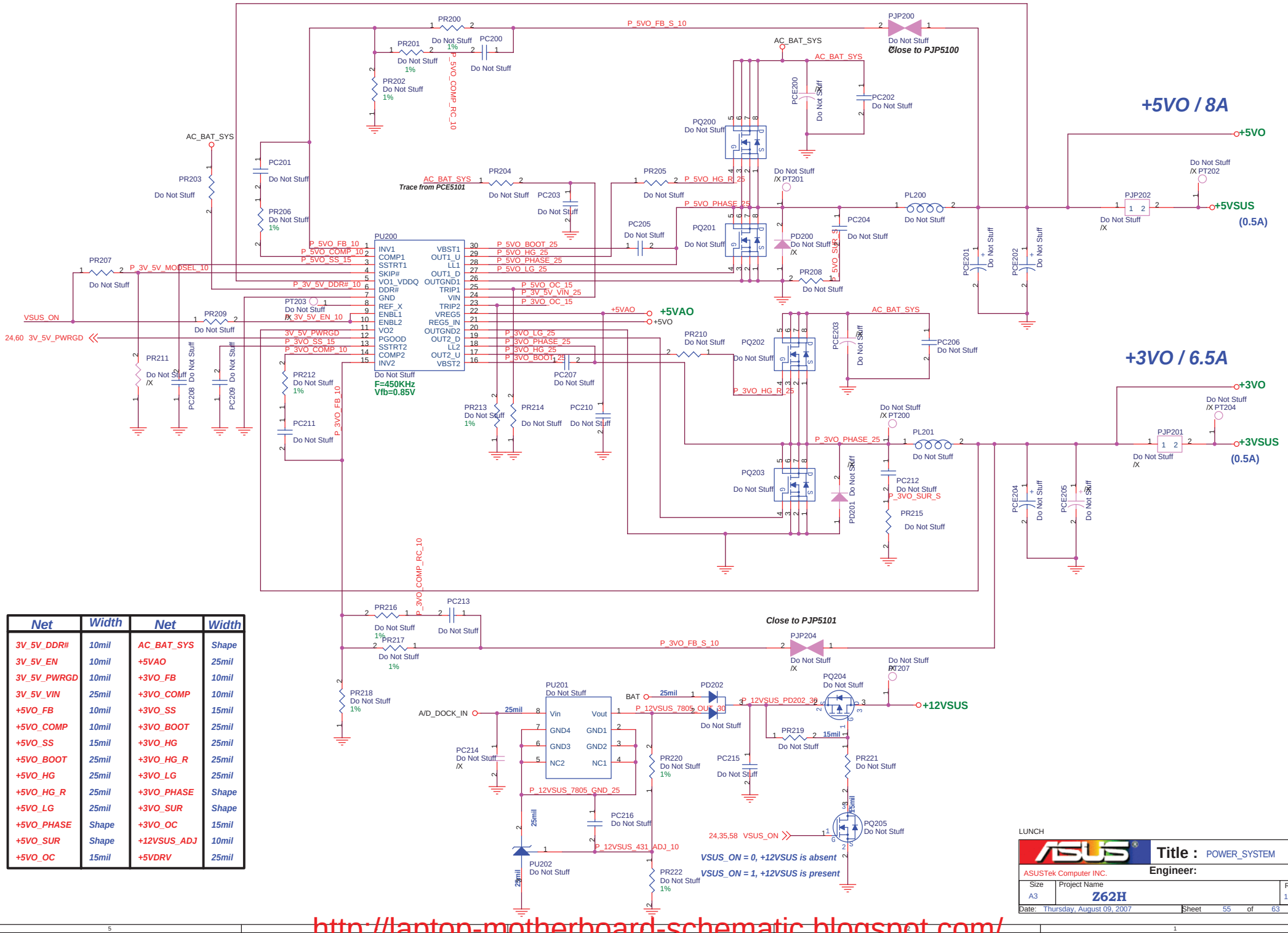
ASUSTek Computer INC.

Title : POWER_CHARGER

Engineer:

Size: C | Project Name: Z62H | Rev: 1.0

Date: Thursday, August 09, 2007 | Sheet 54 of 63



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

LUNCH

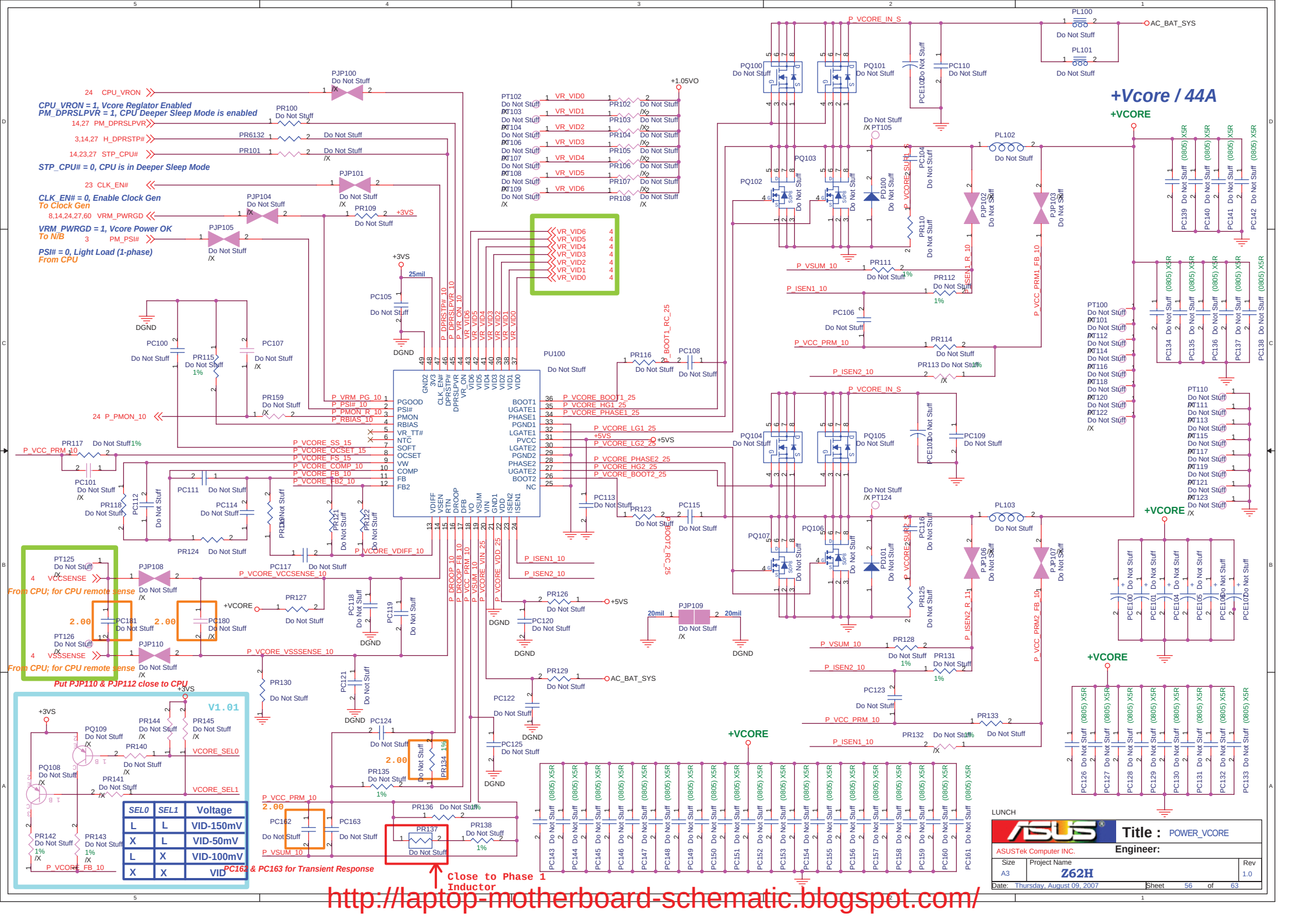
ASUSTek Computer INC.

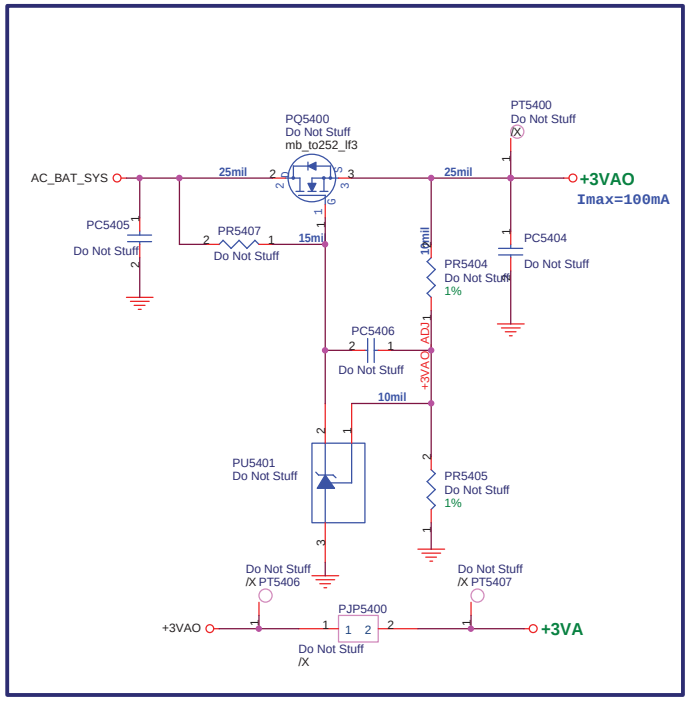
Title : POWER_SYSTEM

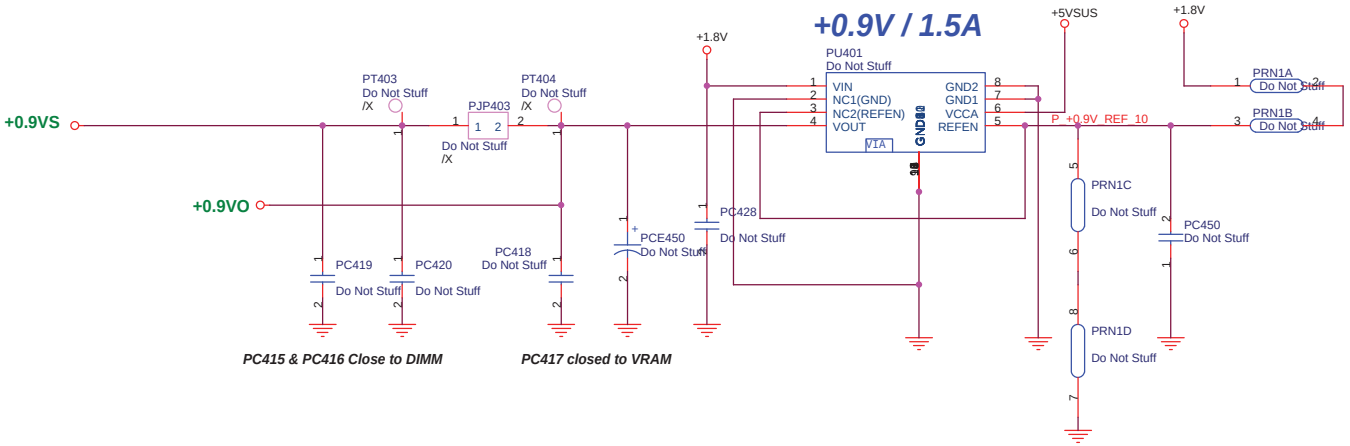
Engineer:

Size	Project Name	Rev
A3	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 55 of 63


+Vcore / 44A
+VCORE
CPU_VRON = 1, Vcore Reglator Enabled
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
STP_CPU# = 0, CPU is in Deeper Sleep Mode
CLK_EN# = 0, Enable Clock Gen
To Clock Gen
VRM_PWRGD = 1, Vcore Power OK
To N/B
PSI# = 0, Light Load (1-phase)
From CPU
From CPU; for CPU remote sense
Put PJP110 & PJP112 close to CPU
PC162 & PC163 for Transient Response
Close to Phase 1 Inductor
V1.01
SEL0 SEL1 Voltage
L L VID-150mV
X L VID-50mV
L X VID-100mV
X X VID
LUNCH
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer:
Size A3
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 56 of 63
http://laptop-motherboard-schematic.blogspot.com/

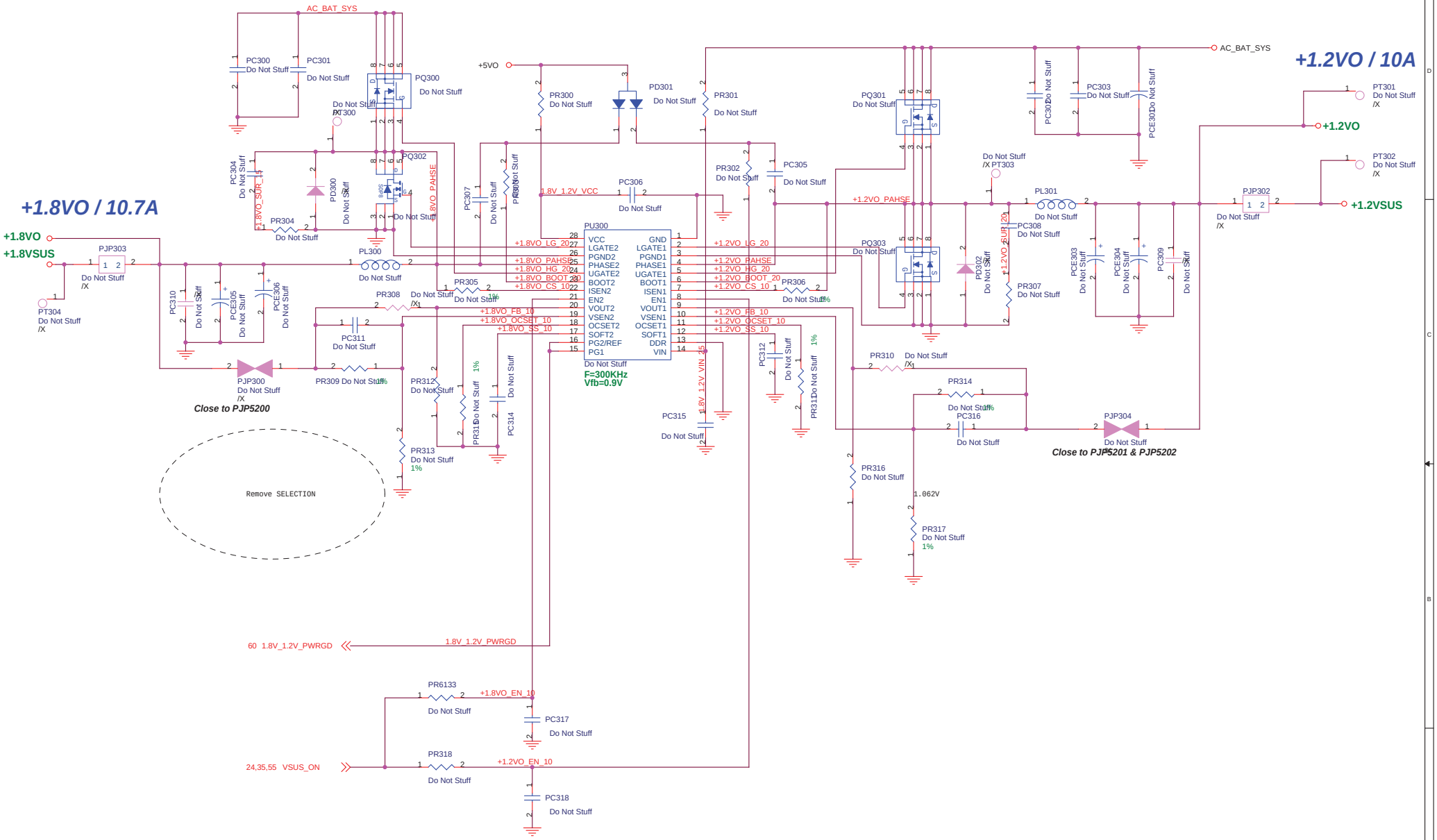




DDR Power Rev:1.00

LUNCH

ASUSTek Computer INC.	Title :	
	Engineer:	
Size: A3	Project Name	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 57 of 63	



LUNCH

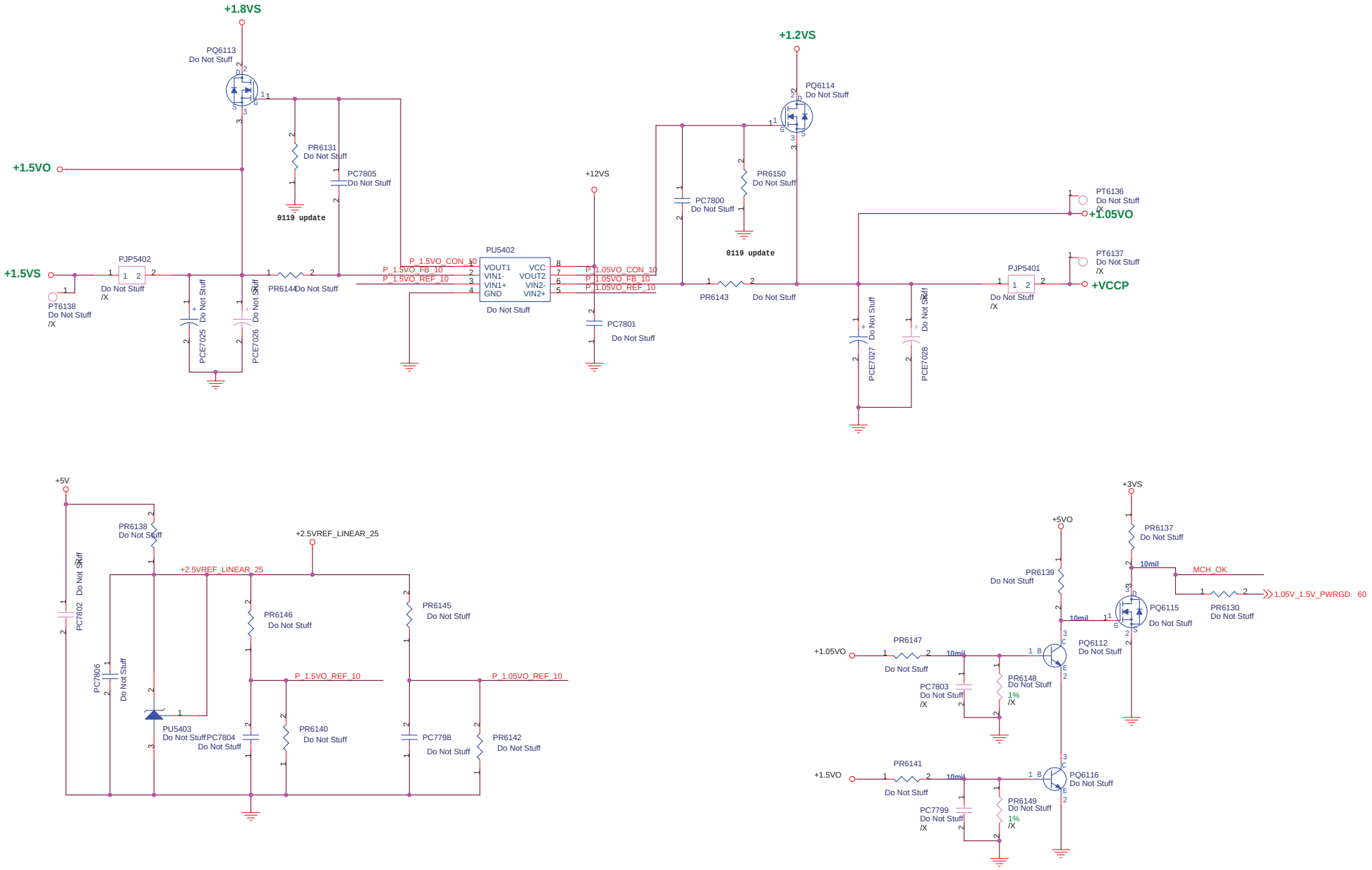
ASUSTek Computer INC.

Title : POWER_I/O_1.5VS & 1.05VS

Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

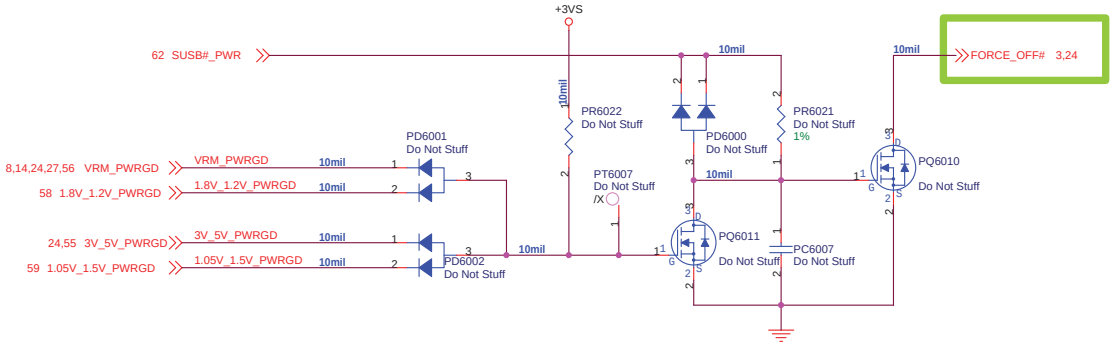
Date: Thursday, August 09, 2007 Sheet 58 of 63

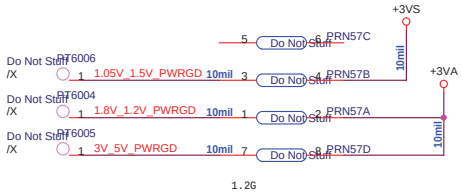


LUNCH

ASUSTek Computer INC.	Title : POWER_I/O_+3VA & +2.5V	
	Engineer:	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 59 of 63	

Power Good Detecter





1.26

LUNCH

ASUSTek Computer INC.	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Friday, August 10, 2007	Sheet 60 of 63	

LUNCH

Title : POWER_BLANK

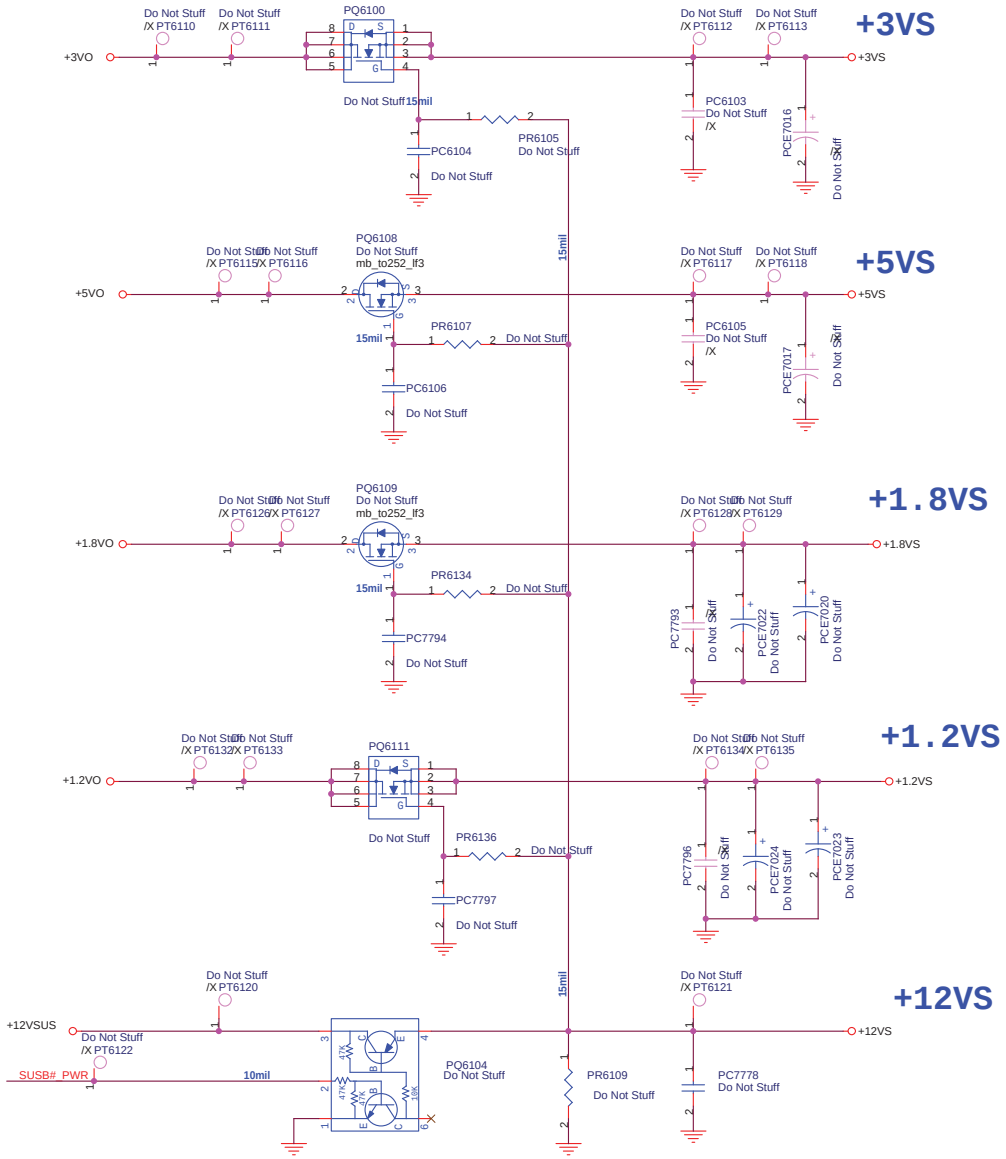
ASUSTek Computer INC.

Engineer:

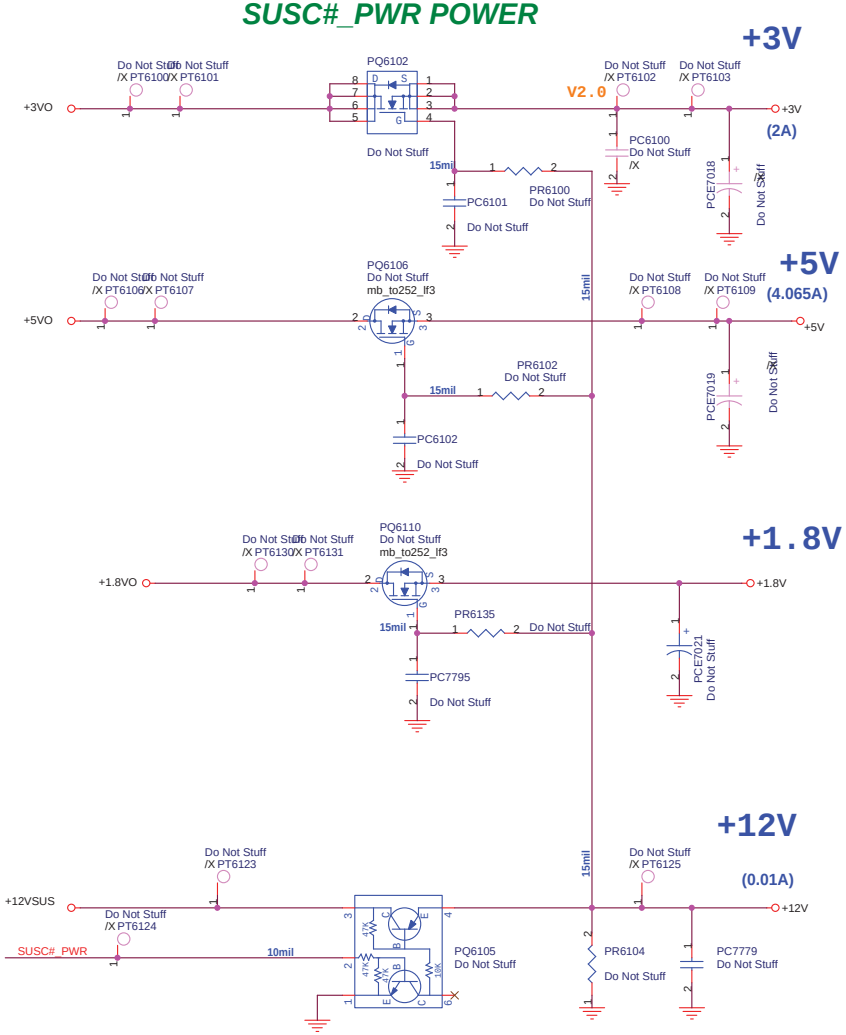
Size	Project Name	Rev
Custom	Z62H	1.0

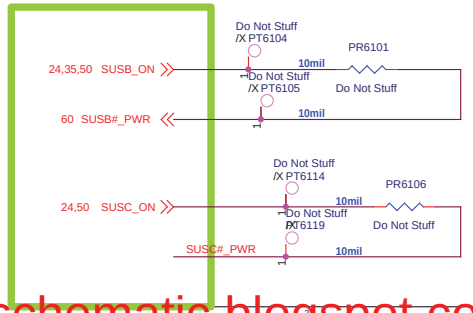
Date: Thursday, August 09, 2007 Sheet 61 of 63

SUSB#_PWR POWER



SUSC#_PWR POWER





LUNCH

ASUSTek Computer INC.

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 62 of 63

Rev	Date	Description
1.0	2007/02/14	1. Initial release.
1.1	2007/05/29	1. Change to SiSM672, SiS968, SiS307

Rev	Date	Description

LUNCH

ASUSTek Computer INC.

Title : History

Engineer: Chihwan

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 63 of 63